International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459 (Online), An ISO 9001:2008 Certified Journal, Volume 3, Special Issue 1, January 2013)
International Conference on Information Systems and Computing (ICISC-2013), INDIA.

EFFICIENT DESIGN OF EDDR CIRCUIT FOR ADVANCED VIDEO CODING/H.264

Rini Franklin. F[1], Prakash. P[2]

[1] PG Student, ME Computer and Communication, Sri Sai Ram Engineering College, Chennai 44, India;
[2] Assistant Professor, Department of IT, Sri Sai Ram Engineering College, Chennai 44, India.

[1]rinifranklin@gmail.com
[2]prakesh.IT@sairam.edu.in.

Abstract

Advanced video coding/H.264 is the video compression standard introduced by ISO/IEC. Motion Estimation (ME) has a critical role in the video coder. The main objective of Motion Estimation is to exploit temporal correlation among adjacent frames in a video sequence to reduce redundancy. Testing such a module is of priority concern. Processing Equipments (PEs) are the key components of Motion Estimation (ME). An error in PE affects the visual quality and PSNR (peak signal to noise ratio) of the high definition video. The error can be detected and recovered effectively by using proposed Error Detection and Data Recovery (EDDR) design based on Residue and Quotient (RQ) code. The proposed EDDR have acceptable area overhead and time penalty. Thus the reliability and throughput of Motion Estimation will be improved.

***Keywords*- Area overhead, Error Detection and Data Recovery, Motion Estimation, Processing Equipment, Residue and Quotient code.**

I. INTRODUCTION

Video compression reduces storage space and increases transmission capacity. It is used in a wide range of applications. A new video coding standard called MPEG4 [Part-10] was developed by Video Coding Experts Group (VCEG) and Moving Picture Experts Group (MPEG). MPEG4 [Part-10] is also called Advanced video coding (AVC) or H.264. Comparing the AVC/H.264 with MPEG 4 [Part 2], H.263 and MPEG-2, the new standard can achieve 39%, 49%, and 64% of bit rate reduction respectively. AVC requires only one third of the original bandwidth and can provide same as MPEG-2 quality. AVC support variable block sizes for motion compensation. The video sequence hierarchy is given by, sequence (pictures (slices (macro blocks (sub-macro block (blocks (samples))))))). The seven different sizes of prediction partitions are 16x16, 16x8, 8x16, 8x8, 8x4, 4x8 and 4x4. In past standards, motion compensation used entire macro blocks, but in the AVC have the largest variety of partition shapes provided enhanced prediction accuracy and increases the compression ratio.

In recent years, multimedia application has become more flexible and powerful with the development of semiconductors, digital signal processing, and communication technology. Advance Video Coding is regarded as the next generation video compression standard.

For video coding systems, motion estimation is the most computationally demanding components in a video encoder. ME is of priority concern in exploiting the temporal redundancy between successive frames. In video coder 60% to 90% of the total of computation time is consumed in motion estimation. The motion estimation algorithm used also profoundly influences the visual quality of reconstructed images. More accurate predictions increase the compression ratio and improve peak signal to noise ratio (PSNR) at a given bit rate.

A ME generally consists of processing equipments with a size of 4x4. If an error occurred in the ME process then the visual quality and peak signal to noise ratio at a given bit rate are greatly influenced. With the advent of VLSI technologies large number of PEs of a ME is integrated into a chip, the logic per pin ratio is subsequently increased, thus decreasing significantly the efficiency of logic testing of the chip. As a commercial chip, it is necessary for the ME to introduce design for testability (DFT). There are many approaches to DFT, which can be divided into three categories Adhoc, structured and BIST. Among them, BIST has obvious advantages because there is no need to buy expensive test equipment, like Automatic Test Equipment, so it can efficiently reduce the test cost. BIST for the ME does not expensive test equipment, ultimately lowering test costs. Thus, extended schemes of BIST referred to as built in self diagnosis and built in self correction have been developed recently.

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459 (Online), An ISO 9001:2008 Certified Journal, Volume 3, Special Issue 1, January 2013)
International Conference on Information Systems and Computing (ICISC-2013), INDIA.

In general, BIST technique refers to the capability of a chip board, or system to test itself. The goal of BIST is to add components to a design that will allow it to test itself. Generally, three parts are added to the circuit under test (CUT) to achieve BIST design are test pattern generator (TPG), output response analyzer (ORA) and test controller. The reliability of numerous PEs in a ME can be improved by enhancing the capabilities of concurrent error detection (CED). Thus, based on the CED concept, In this work we develop a novel EDDR architecture based on the RQ code to detect errors and recover data in PEs of a ME and, in doing so, further guarantee the excellent reliability for video coding testing applications.

II. Related Work

Video is the sequence of still frames. There are two kinds of frames, intra frame and inter frame. The intra frame has no reference frame, so it is encoded separately. In the inter frame previous or successive frame can be a reference frame. Only the difference between the current frame and the reference frame is encoded. Variable block size motion compensation has become an important video coding technique. It has been adopted by the emerging video coding standard H.264. The motion characteristic in a macro block is more accurately represented and therefore, reduces the prediction error to achieve a high compression ratio. It causes high computational complexity in motion estimation at the encoder. H.264 encoder uses a fast inter mode decision algorithm. Using likelihood and correlation of motion field a suitable block mode is selected. This method reduces a considerable amount of complexity at encoder [1], [2].

H.264 permits more than one reference frame for increased precision in motion estimation**.** A suitable reference frame is selected by smart selection mechanism. Then only the selected frames will be searched further in the variable block size motion estimation. Context based adaptive criteria is used to determine whether it is necessary to search more reference frames[3],[4],[5].Concurrent Error Detection(CED) can also test the circuit at full operating speed without interrupting a system [6].

Motion estimation is computationally intensive part of video coder, testing of such high complexity and high density circuits becomes very difficult and expensive.Thus, architecture design of ME requires the design for testability (DFT), DFT focuses on increasing the ease of device testing, thus guaranteeing high reliability of a system. DFT methods relay on reconfiguration of a circuit under test (CUT) to improve testability but it increases the test cost [7], [8].

Among the DFT approaches, BIST has obvious advantages in that reduces the need for expensive external test equipment, Since circuit and tester are implemented in the same chip [9], [10]. Thus EDDR architecture based on the RQ code is designed to detect errors and recovery data in Processing Equipments of a Motion Estimation.

III. Proposed Work

The conceptual view of the proposed EDDR scheme, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data in a specific CUT. The test code generator (TCG) utilizes the concepts of RQ code to generate the corresponding test codes for error detection and data recovery. In other words, the test codes from TCG and the primary output from CUT(Circuit Under Test) are delivered to EDC to determine whether the CUT has errors. DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to export error free data or data recovery results.

The error in the processing equipments (PEs), a key component of ME can be detected and recovered effectively using EDDR design. The input data of Current pixel and Reference pixel are sent simultaneously to PEs and TCGs. The output of PEs is the Absolute difference (AD) between the Current pixel and Reference pixel. The input given to PE1 and TCG1 will be the same, PE2 equal to TCG2 and so on. An error will be occurring in the PEs while calculating absolute difference value. PE1 absolute difference value is selected by selection line S1 of MUX1 and given to the RQCG circuit in order to generate R_{PEi} and Q_{PEi}.

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459 (Online), An ISO 9001:2008 Certified Journal, Volume 3, Special Issue 1, January 2013)
International Conference on Information Systems and Computing (ICISC-2013), INDIA.

An error will be occurring in the PE can incur errors in computing AD values, so this error will be reflected while calculating the R_{PEi} and Q_{PEi} .TCG is the combination of PE and RQCG which produce R_{Ti} and $Q_{T,}$ Meanwhile, the corresponding test codes R_{Ti} and Q_{Ti} from a specify TCG_i are selected simultaneously by MUXs 2 and 3 respectively.

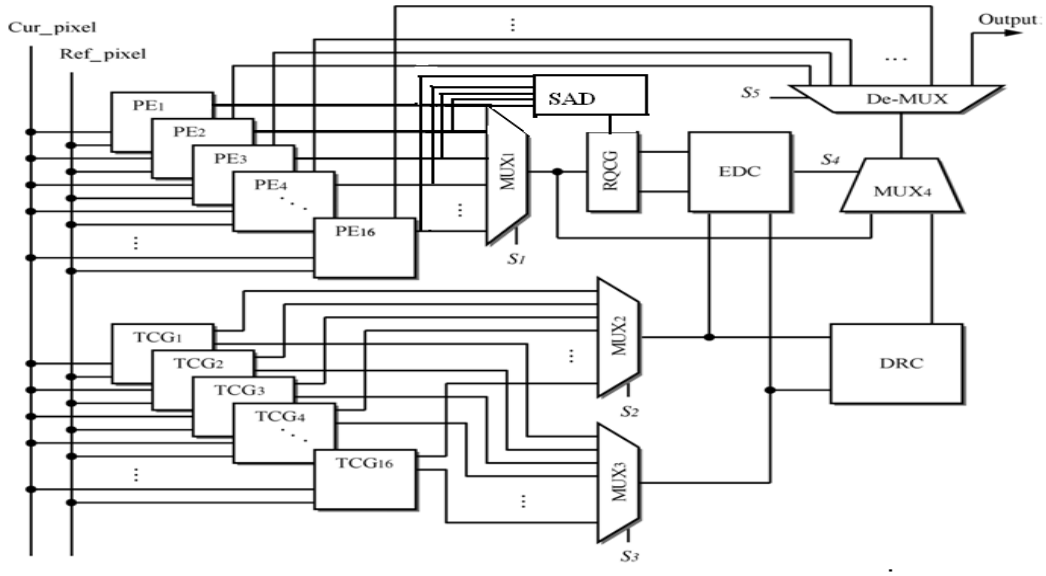

Fig . 1. Proposed EDDR architecture design for a Motion Estimation

The RQ code from TCG_i and RQCG circuits are compared in EDC to determine whether the tested object PE_i have errors. The control signal S_4 is generated from EDC, indicating that the comparison result is error free (S_4=0) or if error (S_4=1) . The tested object PE_i is error free if and only if $R_{PEi} = R_{Ti}$ and $Q_{PEi} = Q_{Ti}$. If error occurs data recovery circuit is used to recover data from TCG_i. The error free data or data recovery results are selected by MUX 4. Finally, the error free data or the data recovery result from the tested object PE_i is passed to a DeMUX, which is used to test the next specific PE_{i+1} otherwise, the final result is exported. It is shown in the Fig. 1.

3.1 Fault Model

The stuck at fault is a logical fault model that causes the line in the circuit to be struck at logic 0 or logic 1. The SA fault in a ME architecture can incur errors in computing SAD values. A distorted computational error (e) and the magnitude of are assumed here to be equal to AD^I –AD in PEs, where AD^I denotes the computed AD value with SA faults.

3.2 Sum of absolute differences (SAD)

Sum of absolute differences (SAD) is a simple algorithm for measuring the similarity between Image blocks.

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459 (Online), An ISO 9001:2008 Certified Journal, Volume 3, Special Issue 1, January 2013)
International Conference on Information Systems and Computing (ICISC-2013), INDIA.

The absolute difference between each current pixel and the corresponding reference pixel in the original block and the block used for comparison is calculated. The differences are summed to create a simple metric of block similarity.

A numerical example of the 16 pixels for a 4X 4 macroblock in a specific PEi of a ME is described. An example of pixel values of the Cur_pixel and Ref_pixel. Based on, the SAD value of the 4X 4 macroblock of Fig.2. is

$$SAD = \sum_{i=0}^{3}\sum_{j=0}^{3} |X_{ij} - Y_{ij}| \quad (1)$$

$$= |X_{00} - Y_{00}| + |X_{01} - Y_{01}| + \ldots + |X_{33} - Y_{33}|$$

$$=(128-1)+(128-1)+\ldots\ldots\ldots+(128-5)$$

$$=2124$$

	0	1	2	3
0	128	128	64	255
1	128	64	255	64
2	64	255	64	128
3	255	64	128	128

Cur_pixel

	0	1	2	3
0	1	1	2	3
1	1	2	3	4
2	2	3	4	5
3	3	4	5	5

Ref_pixel

Fig.2. Example of pixel values.

3.3 Processing Equipment

Processing Equipment is used to the calculate Absolute Difference between the current pixel and reference pixel. The pixel value of video will be between 0-255, so the current pixel and the reference pixel value will be a 8 bit number. In the fig.3. two eight bit number 00000111 (7) and 1111111 (255) absolute difference are calculated using the complementary method. It is shown in the Fig.3.

3.4 RQ Code Generation

Residue code is generally separable arithmetic codes by estimating a residue for data and appending it to data. However only a bit error can be detected based on the residue code.

Additionally, an error cannot be recovered effectively by using the residue codes. Therefore, this work presents a quotient code, which is derived from the residue code, to assist the residue code in detecting multiple errors and recovering errors. Assume that binary data Y is expressed as

$$Y = \{ b_{n-1}\ b_{n-2} \ldots\ldots\ b_2\ b_1\ b_0 \} \quad (2)$$

In the RQ code R=X modulo m and Q=X/m respectively. $m = 2^k-1$, where k is equal to n / 2, n is the number of bits in Sum of absolute difference Value (SAD).The number of bits in the SAD is 2124 i.e 12, k=12/2=6, $m=2^6-1=63$.

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459 (Online), An ISO 9001:2008 Certified Journal, Volume 3, Special Issue 1, January 2013)
International Conference on Information Systems and Computing (ICISC-2013), INDIA.

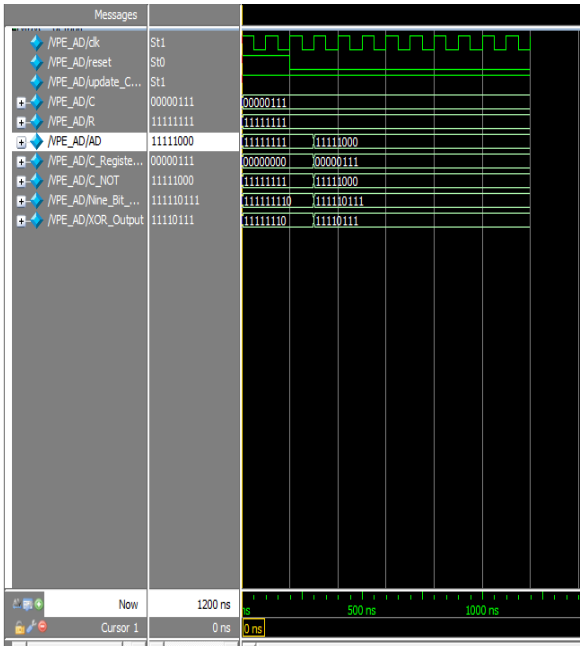

Fig. 3. Time chart of processing equipment

3.5 Test Code Generation

TCG design is based on the ability of the RQCG circuit to generate corresponding test codes in order to detect errors and recover data.TCG is the combination of PE and RQCG.It will produce R_T and Q_T value and given to EDC circuit to detect errors.In the existing system residue and quotient value are found in a separate circuit. It produces residue and quotient value only in 22 clock cycles. Division can be done by continuous subtraction. We can use a combination of subtraction unit and calculate residue and quotient value in reduced clock cycles, so the testing time will be greatly reduced.

3.6 EDDR Circuit

The outputs between TCG and RQCG is compared in EDC (Error Detection Circuit) in order to determine whether errors have occurred. If the values of $R_{PE} = R_T$ and $Q_{PE} = Q_T$, then the errors in a specific PE can be detected. The EDC output is then used to generate a 0/1 signal to indicate that the tested PE is error free/errancy.

DRC (Data Recovery circuit) is in charge of recovering data from TCG.

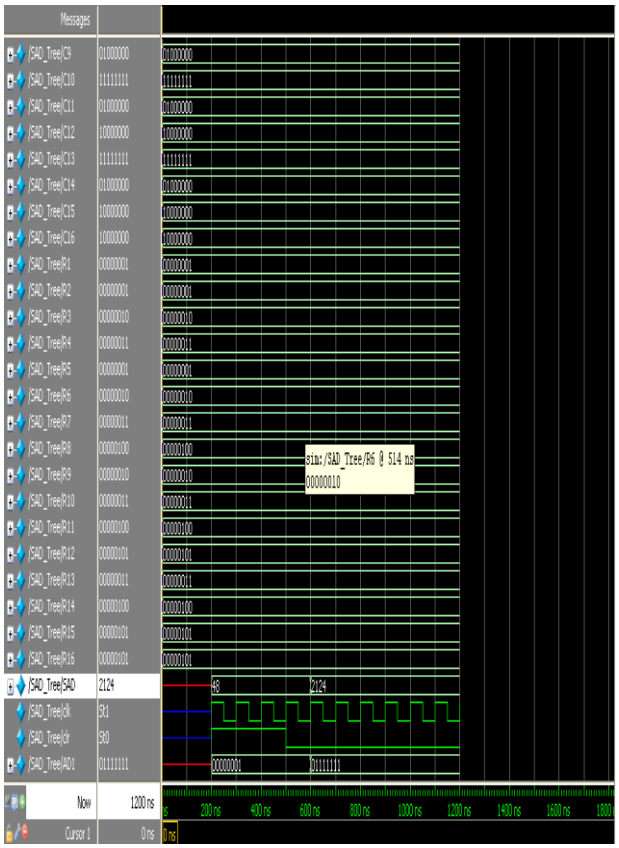

Fig. 4. Time chart of Sum of Absolute Difference

IV. CONCLUSION

In this work EDDR circuit is designed for detecting the errors and recovering the data of PEs in a ME. The proposed EDDR architecture is also implemented by using Verilog and synthesized by the ModelSim and Xilinx.The EDDR circuit is designed with reasonable area overhead and only a slight time penalty.The complexity of RQCG code generation is decreased so testing time is greatly reduced. Throughput and reliability of Motion estimation will be increased.

REFERENCES

[1] Tien-Ying Kuo, and Chen-Hung Chan, " Fast Variable Block Size motionEstimation for H.264 Using Likelihood and Correlation of Motion field", IEEE Transactions on circuits and systems for video Technology Vol. 16, No. 10, October 2006.

[2] C. Y. Chen, S. Y. Chien, Y. W. Huang, T. C. Chen, T. C. Wang, and L. G. Chen, "Analysis and architecture design of variable block-size motion estimation for H.264/AVC," IEEE Trans. Circuits Syst. I,Reg.Papers, vol. 53, no. 3, pp. 578–593, Mar. 2006.

[3] Tien-Ying Kuo, *Member, IEEE*, and Hsin-Ju Lu, "Efficient Reference Frame Selector for H.264," IEEE Transactions on circuits and systems for video Technology, VOL. 18, NO. 3, MARCH 2008.

[4] Y. W. Huang, B. Y. Hsieh, S. Y. Chien, S. Y. Ma, and L. G. Chen,"Analysis and complexity reduction of multiple reference frames Motion estimation in H.264/AVC," IEEE Trans. Circuits Syst.Video Technol., vol. 16, no. 4, pp. 507–522, Apr. 2006.

[5] Hasan F. Ates, and Yucel Altunbasak," Rate-Distortion and Complexity Optimized Motion Estimation for H.264 Video Coding "IEEE Trans. Circuits Syst. Video Technol., VOL. 18, NO. 2,FEBRUARY 2008.

[6] S. Bayat Sarmadi and M. A. Hasan, "On concurrent detection of errors in polynomial basis multiplication," IEEE Trans. Vary Large Scale Integr. (VLSI) Systs., vol. 15, no. 4, pp. 413–426, Apr. 2007

[7] M. Y. Dong, S. H. Yang, and S. K. Lu, "Design-for-testability techniques for motion estimation computing arrays," in Proc. Int. Conf.Commun., Circuits Syst., May 2008, pp. 1188–1191

[8] Y. S. Huang, C. J. Yang,"C- testable motion estimation design for video coding systems," J. Electron. Sci. Technol., vol. 7, no.4, pp. 370–374, Dec. 2009.

[9] D. Li, M. Hu, and O. A. Mohamed, "Built -in self-test design of motion estimation computing array," in Proc. IEEE Northeast Workshop Circuits Syst., Jun. 2004, pp. 349–352.

[10] Y. S. Huang, C. K. Chen, and C. L. Hsu, "Efficient built-in self-test for video coding cores: A case study on motion estimation computing array," in Proc. IEEE Asia Pacific Conf. Circuit Syst., Dec. 2008, pp.1751–1754.