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SIGNAL DEGRADATION DUE TO VIAS IN MULTILAYER PCBs

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Abstract

The design of PCB a high speed digital is high value of signal integrity in the reduction of losses, noises and interference phenomenon below certain levels, because they adversely affects the signal quality. System interference includes SSN, Crosstalk, Jitter, Skew, EMI and interconnects failure includes lossy lines, radiations of vias etc. In this paper signal quality is measured after the via of a multilayer PCB, signal measurement are done, using eye patterns both in the input and output ports. The study shows that there is a change in rising and falling edges of the signal pulses causing eye opening to change.

***Index Terms*- Multilayer PCBs, Vias, Eye diagram, EMI, Signal Integrity**.

I. INTRODUCTION

The digital circuits of the current era is operating on vary high speed of signals varying from several Gbps to Tbps. For this speed a lot to discuss on the signal quality, such as signal speed, transmission line parameters, drivers, power supply, ground plane, EMI, radiation, losses etc. In printed circuit boards (PCBs) the components are operating at different frequencies.

The performances of electronic products and systems are adversely affected by physical damage to interconnect across which signal travels. Common interconnects at the circuit board levels include, solder joints, PCB traces, component leads, convertors and vias [1]. In multilayer PCBs, a signal may be transmitted over vias of different layers to avoid the layer crossing. Due to effects of layer spacing the transmission lines and traces are to be placed to avoid reflections. The transmission lines are left unterminated or improperly terminated the voltage level on the line will generate signal distortions.

Model of Vias-

Vias are transmission lines that pass through different layers of multilayer PCBs and connect two different layers. A through-hole type of via is more commonly used in circuits.

The equivalent circuit element is shown in Figure.1 and Figure 2.

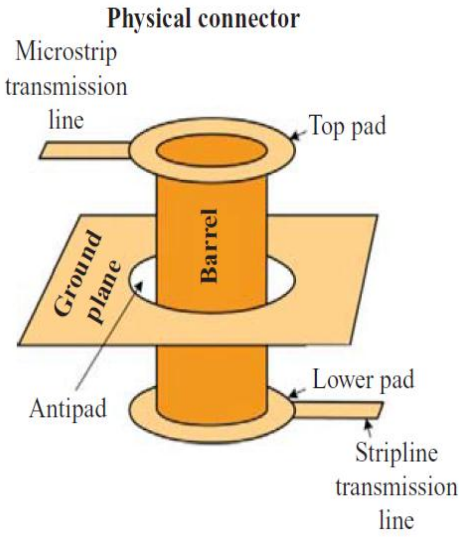

Figure 1: Physical Via

According to MIL STD-275 E, the through-hole diameter for standard packing of T/4, where T is the board thickness.

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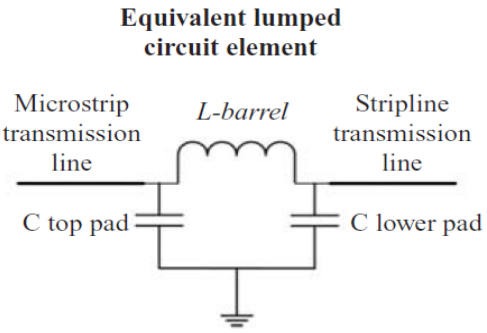

Figure 2: Lumped model of Via

Capacitance of Vias

Every Via has a parasitic capacitance to groung. The parasitic capacitance for a via is calculated as-

$$C = \frac{1.41\epsilon_r T D_1}{D_2 - D_1}$$

Where D_1 – diameter of pad surrounding via, in.

D_2 – diameter of clearance hole in ground plane(s), in.

T – thickness of PCB, in.

ϵ_r – relative electric permeability,

C – parasitic via capacitance, pF.

The primary effects of Via capacitance is that it slows down or degrades the rising edges of digital signals.

Inductance of Vias

Inductance OF Vias is more important than that of capacitance to high speed design. It also degrades the signal quality. The magnitude of the inductance is given as

$$L = 5.08h\left[ln\left[\frac{4h}{d}\right] + 1\right]$$

Where L= inductance of via, nH.

h= length of via, in.

d= diameter of via, in.

The combined effect of parasitic capacitance and Inductance affects the rising and falling edges of a digital signal.

II. ANALYSIS

We are taking for the signal analysis a conventional via of height 0.625mm, dia of 0.375mm, thickness of 0.00375mm. Two vias of equal distance are connected by a trace, of width 0.625mn for a length of 4.1mm. The transmission lines are at layer 1 and trace at layer 3. Layer4 is considered as ground plane. The layout is shown in Figure 3.

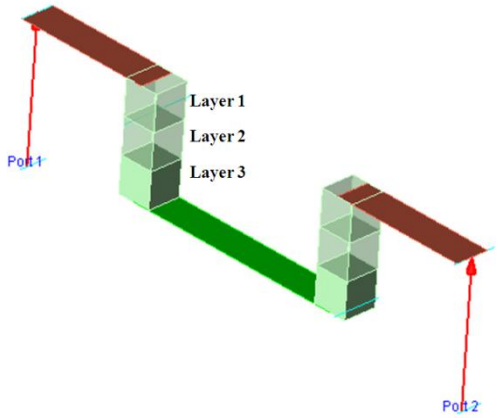

Figure 3: PCB layer with Via

The eye diagram analysis is carried out using ADS tool, for a signal transmission of bits at a data rate of I Gbps and a rise/fall time of 100ps. The eye diagram for ideal case is shown in Figure 4.

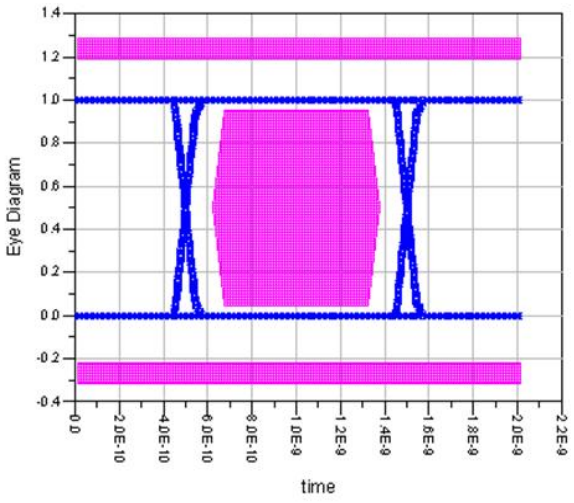

Figure 4: Eye Pattern for Ideal case

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The Eye diagram for the PCB with Via transition is shown in following Figure 5. It is observed that the change occurs in the Eye opening Rise and fall times of the signal.

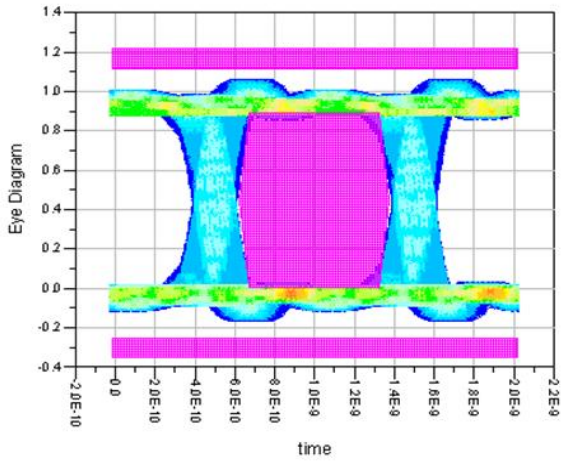

Figure 5: Eye Pattern after via placement

III. Signal Integrity Analysis

The variation in rise and fall times affects the signal at the receiving end. This is due to the distortion caused by vias over the signal transmission. This distortion can be mitigated using various techniques such as implementing EBG layers etc.

IV. Acknowledgement

The authors would like to thank Mr.T.Jayanandan, Communications system Engineer for developing the Eye diagram

V. Conclusion

In this work the signal distortion is analyzed for multilayer PCBs with vias. Due to the presence of vias the signal is distorted from its ideal value to a distorted value. This effect can be rectified using various techniques.

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