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FPGA Implementation of Switching System Using VHDL

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Abstract

In this paper, we focuses on the programming part as well as the hardware, thus proving a step towards the future development of 'Switching ICs'. Here we explain every model in detail with their opcodes (user defined), underlying architecture and programming. Along with are also provided the simulation results showing transfer of signals and data. Simulator also provides the timing information. This paper is an outcome of the comprehension and utilization of many recent subjects we have studied and is in itself an original concept.

***Keywords*-- FPGA, SS7, VHDL, Switching system, signaling.**

I. Introduction

The transmission of telegraphic signals over wires was the first technological development in the field of modern communications. Telegraphy was introduced in 1837 in Great Britain and in 1845 in France. In March 1876; Alexander Graham Bell demonstrated his telephone set and the possibility of telephony, i.e. long distance voice transmission. Graham Bell demonstrated a point-to-point telephone connection. A network using point-to-point connection is shown below fig.1.

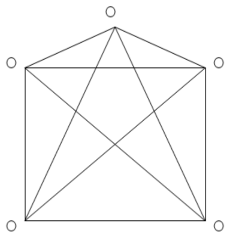

Fig 1. A network with point to point connection

In general case with n entities, there are N (N-1)/2 links, therefore the number of links required with moderate or higher values of n to have fully connected system becomes very large. Consequently, practical use of bell's invention on the large scale or even on the moderate scale demanded not only the telephone sets and the pair of wires, but also the so called the switching system. With the introduction of switching system, the subscribers are not directly to switching system, which results in increment in speed or response and most efficient way to connect the connection. When a subscriber wants to communicate with another a connection is established between the two at the switching system.

In this switching system only one link per subscriber is required between subscriber and switching system and the total no of such links is equal to the number of subscriber connected to the switching system. Earlier switching system were manual and operator oriented. Limitations of operator oriented switching system were quickly recognized and automatic changes came into existence. Automatic switching systems can be classified as electromechanical and electronic. Electromechanical switching system include step by step and crossbar systems the step by step is common known as strowger switching system. The control functions in a strowger switching system are performed by circuits associated with the system. Crossbar systems had hardwired control systems, which uses relays and latches. These systems have limited capability and it is virtually impossible to modify them to provide additional functionalities.

Classification of switching system

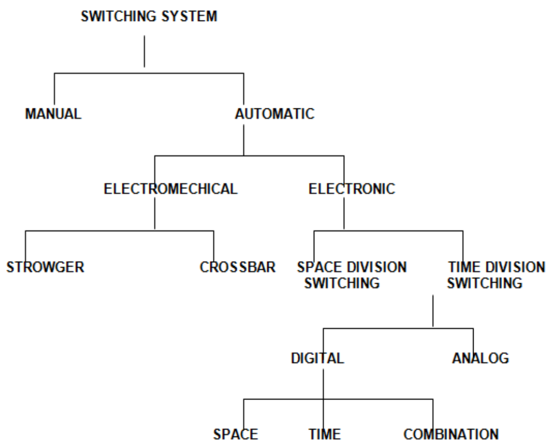

Fig.1

In electronic switching the control functions are performed by a computer or a processor. Hence these systems are called stored program control. The switching system may be either space division switching or time division switching .In space division switching a dedicated path is established between a calling and called subscriber, whereas in time division switching sampled values of speech signals are transferred at fixed time interval. Time division switching may be digital or analog .Digital switching is divided into two parts space switch and time switch. If the coded values are transferred during the same time interval the technique is called space switching. If the values are stored and transferred to the output at a later time interval, the technique is called time switching.

II. Basics Of Switching System

A major component of a switching system or an exchange is the input and output circuits called inlets and outlets. The primary function of the switching system is to establish a path between inlet and outlet. The hardware used is the switching network. If there are N inlets and M, outlets, when N=M the network is called symmetrical network. The inlets and outlets may be connected may be connected to local subscriber or trunk from / to other exchanges .when all inlets and outlets are connected to subscriber lines the logical connection appears, In this case the output lines are folded back to input and hence called the folded network.

Four types of connection can be established:

1. Local call connection between two subscribers in the system
2. Outgoing call connection between an incoming trunk and a local subscriber
3. Incoming call connection between an incoming trunk and a local subscriber
4. Transit call connection between an incoming trunk and outgoing trunk

Principle of Landline Switching

In this design, the data coming in through the inlets are written into the data memory and later read out to the appropriate outlets. The incoming and out coming data is usually in serial form whereas the data are written into and read out of the memory in parallel form. It therefore becomes necessary to perform serial to parallel conversion and parallel to serial conversion at the inlets and outlets respectively.

For convenience, the in and data out parts of the MDR are shown separately for the data memory. Since there is only one MDR a gating mechanism is necessary to connect the required inlet/outlet to MDR. This is done by the in gate and out gate units. The information is not transferred in real time: it is first stored in the memory and later transferred to the outlet. There is a time delay between the acquisition of a sample from an inlet and its delivery to the corresponding outlet. This switching system can be controlled in following three ways:

1. Sequential write/Random read.
2. Random write/Sequential read.
3. Random input/Random output.

In the first two methods of control, the sequential / random read / write operations refer to the read / write operations associated with the data memory. In both these cases, the inlets and outlets are scanned sequentially. In the last case, the inlets and outlets are scanned randomly, and the data memory is accessed sequentially.

Sequential write / random read

In this method the inlets are scanned in the first phase one after another and the data is stored in the data memory sequentially. There is a one to one correspondence between the inlets and the locations of the data memory. The control memory locations contain the addresses of the inlets corresponding to the outlets.

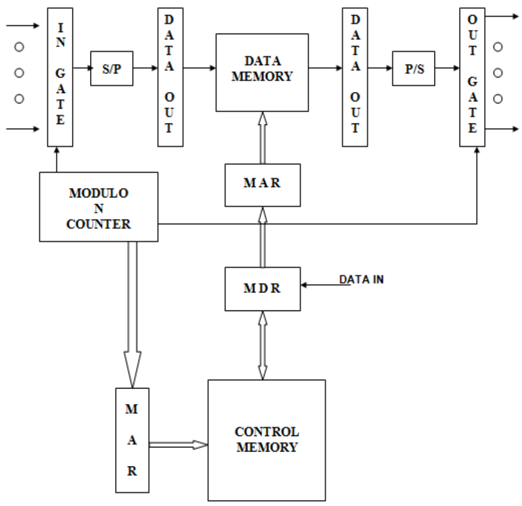

Fig. 2. Switching structure

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The inlet addresses are read out from the control memory in the second phase, the corresponding locations in the data memory are accessed and the data transferred to the outlets in sequence.

Since any inlet may be connected to any of the outlets, the inlet addresses are randomly distributed in the control memory. Consequently, the read access to the data memory is random. Since the write access to the data memory in the first phase proceeds sequentially and the read access in the second phase randomly, the nomenclature sequential write / random read is used to describe this form of control.

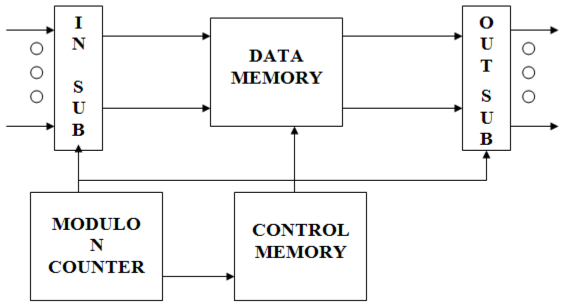

Fig 3. Sequential write / random read

III. LANDLINE SWITCHING IMPLEMENTATION

Specifications:

1. 16 bit opcode

E	I	D 2	D 1	D 0	S 2	S 1	S 0	X	X	X	X	X	X	X	X

2. Interexchange: 8 users in each exchange can communicate with each other
3. Intraexchange: 8 users in one exchange can communicate with each other.
4. Data memory: 9bit of std_logic type (8 locations)
5. Control memory: 8 locations of integer type.
6. Caller id: 8 locations each of 3 bit

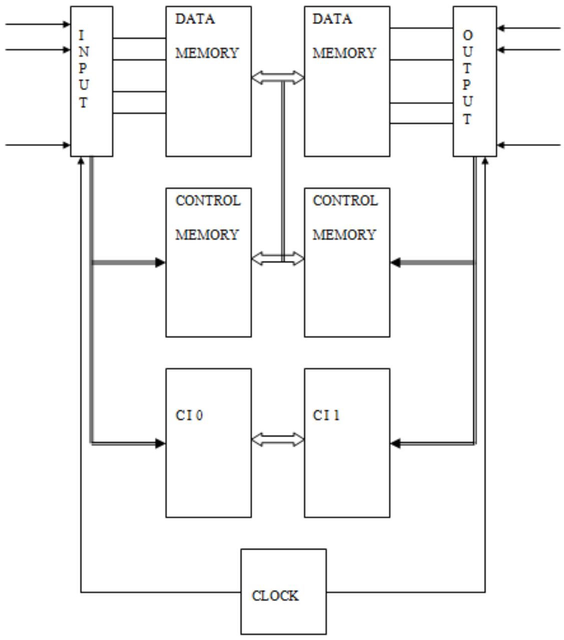

Fig 4. The Landline Switching architecture

IV. WORKING SPECIFICATIONS

Phase 1: Input Subscribers in both the exchanges are scanned sequentially. It takes 8 clock cycles to scan 16 subscribers in order to know their status, that is they want to transmit or not. This is called a sequential scanning. The date to be transmitted is stored in data memory in sequential order. The information relating to the called subscriber is stored in control memory in sequential order and caller id number is stored in the caller id memory in the sale way. Thus we can say system is sequential write.

Phase 2: When all the scanning is finished the location of the data memory is read according to the corresponding location of the control memory. For example, if first location of data memory has data ‘d’ and corresponding location in control memory is 2, this means that ‘d’ will be communicated to the 2^{nd} user of the exchange, thus we can say the system is random read. To decide where the data will be communicated we use a bit in our op code as ‘I’ bit. If ‘I’ =1, then it is interexchange, i.e. the read out data will be given to user of other exchange. Thus communication between the subscriber of two exchanges can be made possible and hence the name interexchange. If ‘I’ = 0, then it is called as intraexchange, i.e. the read out data, will be given to the user of the same exchange. Thus communication between subscribers of the same exchange is made possible, and hence the name Intraexchange.

The exchange between caller id memories is done only if the particular user is enabled. Same is the case with data memory. A particular user is enabled if its opcode 16th bit is 1 and disabled if it is 0.So caller must be enabled and called must be disabled in order to make a call successful. The communication means just to transfer the data (0- 7 bits of opcode) between entities and is shown by overwriting the data bits if called sub=scriber. Caller id facility enables the called user to see who is calling by checking his relevant bits of opcode (13 to 11).

V. Result

In this the simulation is to be done with the help of Modelsim (Mentor graphics) and the result of Phase I & Phase II model is as shown in fig 5.

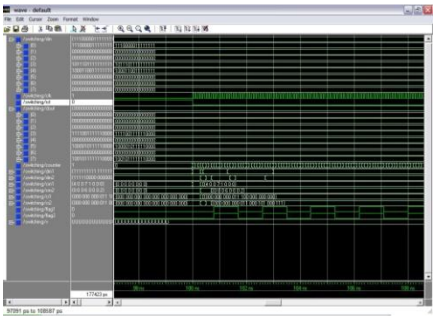

Fig 5. Simulation result of phase I

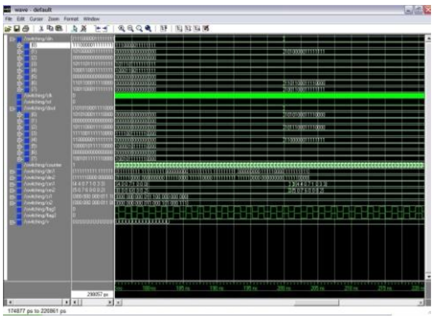

Fig 6. Simulation result of Phase II

VI. Conclusion

The aim of paper was to enable us to design ICs for the Switching System. Presently switching systems uses multiplexers, routers, switches etc that leads to low efficiency as they are analog in nature and have a high power requirement. In contrast we have tried to make this whole system digital to increase the efficiency, lower the power requirement, and reduce the delay. VHDL has been used to write all the programs for the ICs because of its user-friendly nature and thus modifications if required for further development shall not prove to be an obstacle.

As we know, the process of making ICs is time consuming and an expensive venture so we must be sure about the working results of the ICs in advance as we can't accept errors later.

Thus the paper focuses on simulation prior to fabrication. Burning these programs on FPGA (Field Programmable Gate Array) will help us to see the functional design of ICs. These results in addition to the systematic view generated would help us to design Application Specific (AS ICs).

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