International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 4, Special Issue 2, April 2014)
National Conference on Computing and Communication-2014 (NCCC'14)

FPGA Implementation of Vedic Multiplier Using VHDL

A. Wasil Raseen Ahmed
Electronics and Communication Engg, Sona College of Technology, Salem, India

***Abstract*- Processor speed depends mainly on multiplier. It is one of the important blocks in many DSP systems and also in general purpose processors. The multiplier architecture is based on Urdhva Tiryakbhyam (Vertical and Crosswise) Sutra of ancient Indian Vedic mathematics is proposed in this paper. This Sutra (Algorithm) is most efficient in giving minimum delay for multiplication of all types' numbers either small or large. The coding is done in VHDL, Synthesized and simulate using Xilinx ISE series. After the synthesis, Carry Look Ahead Adder (CLAA) is compared with Ripple Carry Adder (RCA) in terms of Path Delay.**

***Index Terms*- DSP, FPGA, VHDL, Vedic Mathematics, Vedic Multiplier, Vertical and Crosswise algorithm.**

I. Introduction

Now a days, the demand of high speed processing has been increasing, the need of high speed multiplier also increasing. Multipliers are mainly used in DSP, Microprocessor, Image processing applications. Time delay and power consumption reductions are essential for many applications. Important fundamental function in arithmetic operation is multiplication. Multiplication based operations such as Multiply and Accumulate (MAC) which is used in many DSP applications such as FFT, filtering etc. The execution time of many Digital signal Processing algorithms depends on multiplication. So there is a need of high speed multiplier .In the past multiplication was implemented generally with sequence of add and shift operations. In digital hardware the most common multiplication algorithm is array multiplication and booth multiplication. In array multiplication the only delay is the time for signal to propagate through the gates. In booth multiplier, large booth arrays are required which in turn require large partial sum and carry registers. The proposed multiplication algorithm based on Vedic mathematics .It's name is from ancient system of Vedic mathematics .The whole of Vedic mathematics is based on 16 sutras (formula). Urdhva tiryakbhyam sutra is in detail.

II. Vedic Multiplier

A. Urdhva Tiryakbhyam algorithm

"Urdhva Tiryakbhyam" (Vertical and Crosswise) sutra (Algorithm).It is a general multiplication formula equally applicable to all cases of multiplication. The algorithm generates all partial product and sum in one step. The algorithm is generalized for nxn bit number .This Multiplier has advantage that when we increase the number of bits ,gate delay and area increases very slowly compared to other multipliers. Due to its regular structure, Multiplier processing power increase by increasing the input and output data bus widths.

B. Multiplication of two decimal numbers 252x846

STEP1

2 5 2
8 4 6
2

STEP 2

Result=12
2 5 2
Pre carry=08 4 6
12 9 2

Result=38
Pre carry=1
39

STEP 3

2 5 2
8 4 6
1 9 2

STEP 4

Result=48
2 5 2
Pre carry=38 4 6
51 3 1 9 2

Result=48
Pre carry=5
53

STEP 5

2 5 2
8 4 6
2 1 3 1 9 2

Result=16
Pre carry=5
21

252x846=213192

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 4, Special Issue 2, April 2014)
National Conference on Computing and Communication-2014 (NCCC'14)

III. PROPOSED MULTIPLIER DESIGN

In the below sections, the hardware architecture of 2x2 and 4x4 Vedic multiplier are displayed. Vertical and crosswise formula is used for such architecture for multiplication of two binary numbers. The specialty of this Vedic multiplier is that addition and partial product generation are done concurrently. Hence it is well suited for parallel processing also. The primary motivation is to reduce the delay.

A. 2 bit Vedic multiplier module.

The method is used for two, 2 bit numbers A and B where A=a1a0 and B=b1b0 as shown in Fig 1.first the LSB are multiplied which gives final product of least significant bit (Vertical).The Least significant bit of multiplicand is multiplied with next higher bit of multiplier and added with product of least significant bit of multiplier and multiplicand of next higher bit (multiplicand).The sum gives the final product of second bit and carry is added with partial product obtained. The third corresponding bit is sum and fourth bit of final product is carry.

$$s0=a0b0; \quad (1)$$
$$c1s1=a1b0+a0b1; \quad (2)$$
$$c2s2=c1+a1b1; \quad (3)$$

The final product is c2s2s1s0.This method of multiplication is applicable to all types.

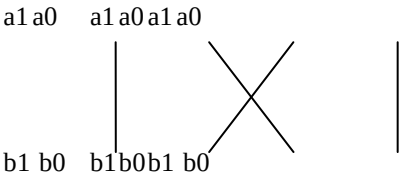


Fig.1 The Vedic Multiplication method for two 2-bit binary numbers

The implementation of 2 bit Vedic multiplier module consists of four input AND gates and two half adders which is shown in Fig 2.The architecture of 2 bit Vedic multiplier is same as the architecture of 2 bit array multiplier. By Vedic method, the multiplication of 2 bit binary numbers does not have significant improvement in multiplier's efficiency. In 2bit Vedic multiplier, the total delay is only 2- half adder delays are same as the array multiplier.

So we move on to the implementation of 4x4 bit Vedic multiplier which is having 2x2 bit multiplier as basic building block.

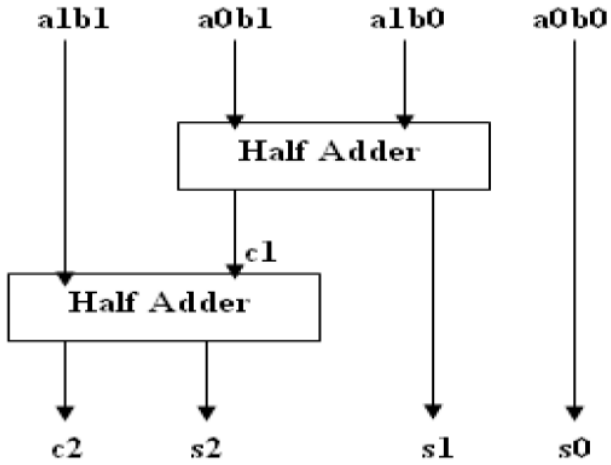


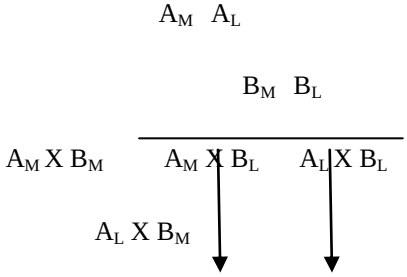
Fig. 2 Block Diagram of 2x2 bit Vedic Multiplier

B. 4 bit Vedic multiplier module.

Analyze the 4x4 multiplication by using $A=A_3A_2A_1A_0$ and $B=B_3B_2B_1B_0$. The final result is $S_7S_6S_5S_4S_3S_2S_1S_0$. Divide A and B into two parts, say A_3A_2 & A_1A_0 for A and B_3B_2 & B_1B_0 for B. With the help of fundamentals of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block.

We can have general representation of multiplication shown in fig below.

For AXB, the general format is



A and B are the multiplicand and multiplier. A_M A_L which represents the parts of A and B as B_M B_L .The block diagram of 4 bit Vedic multiplier is shown in Fig.3 .To get the final product four 2x2 bit Vedic multiplier and three 4-bit Carry Look Ahead (CLA) adders are used.

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 4, Special Issue 2, April 2014)
National Conference on Computing and Communication-2014 (NCCC'14)

The proposed multiplier architecture can used to reduce the delay. In the existing method, Vedic multiplier based on array multiplier structures and also new architecture introduced based on Ripple Carry (RC) adders which help to reduce delay. Reducing time delay essential for many applications. Modification on replacing ripple carry adder to carry look ahead adder. This leads to further delay reduction.

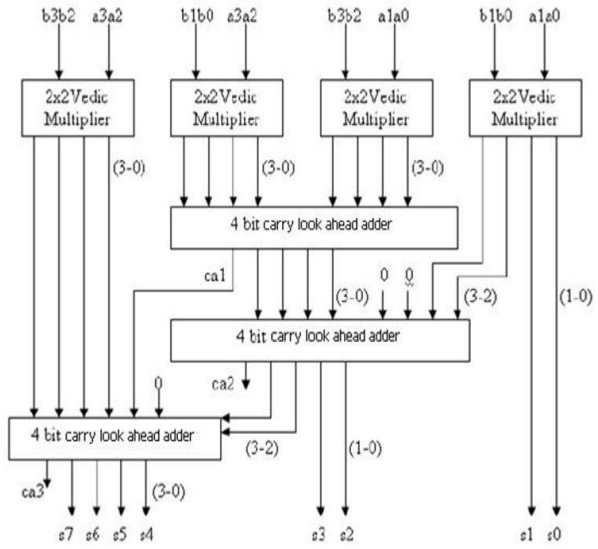


Fig.3 Block Diagram of 4x4 bit Vedic Multiplier

IV. Implementation In XILINX ISE

In this work 4x4 Vedic multiplier is designed using VHDL(Very high speed Integrated Circuits Hardware Description Language),synthesis and simulation was done using XilinxISE9.2i.The circuit performance is evaluated in the Xilinx device family Spartan3,packagetq144 and speed grade-4.

The RTL schematic is shown in Fig.4 and for verification the simulation result obtained shown in Fig.5

a.) For 4x4 bit Vedic multiplier input, the multiplier a=”0001”(decimal number system 1) and multiplicand b=”0010”(decimal number 2) and we get 8 bit output=”00000010”(decimal number system 2)

b.) Again ,we have multiplier a=”0101” (decimal number system 5) and b=”0110” (decimal number system 6) and we get 8 bit output=”00011110”(decimal number system 30).

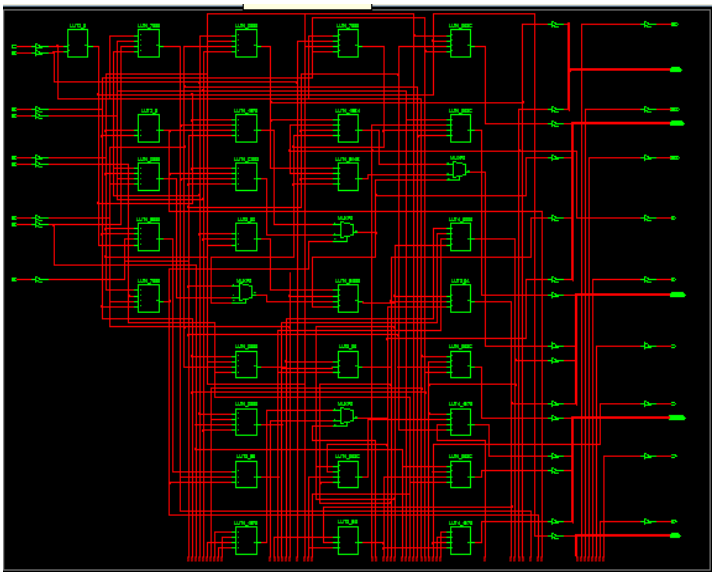


Fig.4 RTL schematic of 4x4 bit Vedic Multiplier

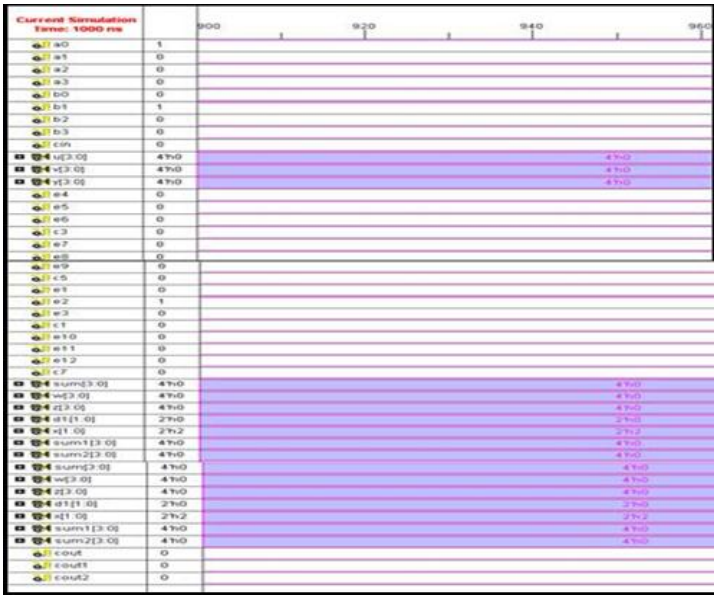


Fig 5 Simulation result for 4x4 Vedic Multiplier

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 4, Special Issue 2, April 2014)
National Conference on Computing and Communication-2014 (NCCC'14)

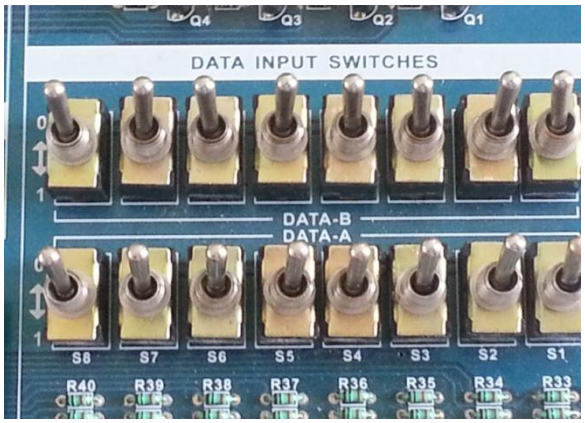


Fig.6 Data Input Switches in FPGA

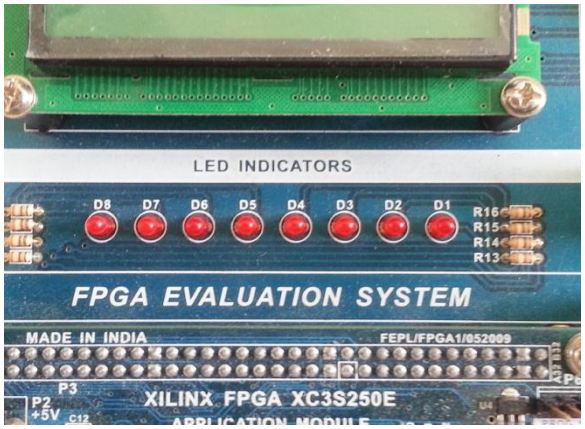


Fig 7 LED Indicators in FPGA

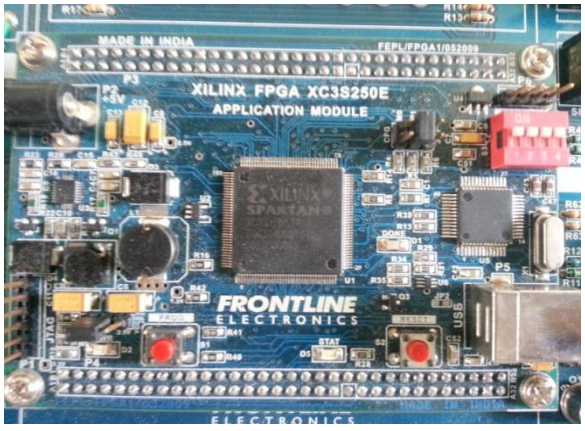


Fig 8 Xilinx FPGA XC3s250E Module

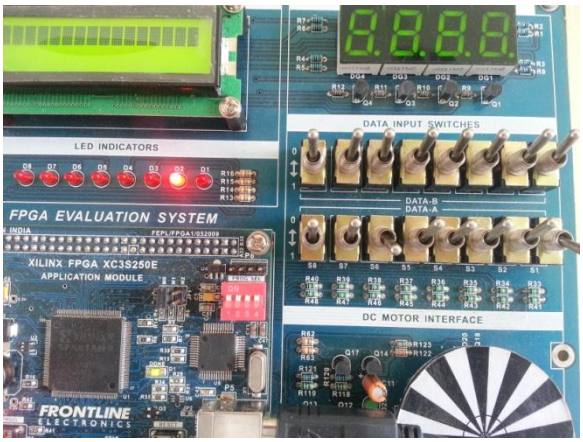


Fig 9 Input and Output in FPGA

In Fig 6 shows the data input switches that will be in off state. In Fig 7 shows LED Indicator where we can get output. In Fig 8 shows the Xilinx FPGA module that is used for this work. In Fig 9 shows Input and Output. Inputs are a=”0001” and b=”0010”. Here Initially a0 is in on state (a0=1) and b1 is in on state (b1 =1) and other values set as ‘0’ that will be displayed in data input switches. The output is displayed in LED Indicators. There are 8 LED Indicators.X0 (1) is in on state(X0(1) =1) and others will be in off state. The Outputs are X0(0), X0(1), Sum2 (0), Sum2 (1), Sum2 (2), Sum2 (3), Cout 1, Cout 2.

V. Result And Discussion

The synthesis result obtained from the Vedic multiplier having Carry Look Ahead adder and Ripple Carry adder .The results are compared .Finally we get Urdhva multiplier with Carry Look Ahead adder is faster than Urdhva multiplier with Ripple Carry adder.

The device utilization summary for proposed 4x4 bit Vedic multiplier for Xilinx, Spartan family is shown below:

Device Utilization summary:

Selected Device: 3s250etq144-5
Number of Slices: 33 out of 960 3%
Number of 4 input LUTs: 59 out of 1920 3%
Number of IOs: 64
Number of bonded IOBs: 64 out of 108 59%

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 4, Special Issue 2, April 2014)
National Conference on Computing and Communication-2014 (NCCC'14)

Table 1 shows the comparison of Urdhva multiplier with Carry Look Ahead adder and Ripple Carry adder in terms of computational path delay in nanoseconds (ns).The timing result shows that Urdhva multiplier with Carry Look Ahead adder is faster than Urdhva multiplier with Ripple Carry adder in terms of execution time.

Table 1
Comparison of 4x4 bit Multipliers (in ns)

Vedic multiplier	Path delay
4x4 Vedic multiplier having Ripple Carry adder	15.995 ns
4x4 Vedic multiplier having Carry Look Ahead adder	13.786 ns

VI. CONCLUSION

A high efficient method of multiplication-"Urdhva Tiryakbhyam Sutra (Algorithm)" based on Vedic mathematics is presented in this paper. It gives the method of hierarchical multiplier design and indicates that computational advantages offered by Vedic methods. The path delay for proposed 4x4 bit Vedic multiplier is found to be 13.786 ns. Our primary motivation is to reduce the delay is finely fulfilled.

Therefore we observe that Urdhva multiplier with Carry Look Ahead adder is faster than Urdhva multiplier with Ripple Carry adder in terms of execution time (speed) and it is also implemented in XilinxISE.DSP algorithms such as Convolution, Fast Fourier Transform, Digital filters etc having multiply accumulate computations. since the multiplication time is faster than addition time, the total processing time of DSP algorithms primarily depends upon number of multiplications. For the future work this multiplier can be used to implement for the above DSP algorithms.

REFERENCES

[1] Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja "Vedic mathematics", 1965

[2] H. Thapliyal and H.R Arbania " a Time-area-Power Efficient Multiplier and Square Architecture based on ancient Indian Vedic mathematics" international conference on VLSI,Las Vegas ,June 2004

[3] S.S kerur "Implementation of Vedic multiplier for DSP", International journal of Technology and Engineering system, Jan 2011

[4] Umesh Akare "performance and evaluation and synthesis of Vedic multiplier", National conference on international paradigms in Engineering & Technology (NCIPET-2012), Jan 2012

[5] Pushpalata Verma, K.K Mehta" Implementation of an Efficient Multiplier based on Vedic Mathematics using EDA Tool", June 2012

[6] Neil H.E Weste, David Harris, Ayan Anerjee,"CMOS VLSI DESIGN, a Circuits and Systems Perspective", Third edition, published by person Education, PP-327-328]