An Another Way for Designing of 4-Bit Carry Skip BCD Adder Using DKFG Reversible Logic gates

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Abstract—At the present time reversible logic is one of the most significant topic and it has different areas for its application. It is very essential to construct low power, low loss computational structures which are very essential for the construction of arithmetic circuits used in nanotechnology, quantum computation and many other low power circuits. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. This paper represents another way for designing of 4-bit carry skip BCD adder using DKFG reversible logic gates. The proposed circuit has a lower quantum cost compared to the other existing circuits.

Keywords—Reversible logic, Basic Reversible Gates, Carry skip BCD, Garbage, Quantum cost, Quantum computing.

I. INTRODUCTION

Energy dissipation is one of the most important considerations in electrical circuit designing. Reversible logic was first related to energy when Landauer states that information loss due to function irreversibility leads to energy dissipation in 1961 who stated that there is small amount of heat dissipation the circuit due to loss of one bit of information and it would be equal to $kT \ln 2$ where ‘k’ is Boltzmann constant and $T$ is the temperature [1]. This principle is further supported by Bennett that zero energy dissipation can be achieved only when the circuit contains reversible gates in 1973. It was proved by Bennett that the energy $kT \ln 2$ would not be dissipate from the circuit if input can be extracted from output and it would be possible if and only if reversible gates are used[2]. According to Moore’s law the numbers of transistors will double every 18 months. Thus energy conservative devices are the need of the day. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information A circuit will be reversible if input vector can be specifically retrieved from output vectors and here is one to one correspondence between input and output [3].

Younis and Knight [4] showed that some reversible circuits can be made asymptotically energy-lossless if their delay is allowed to be arbitrarily large. A reversible logic circuit should have the following features [6]:

- Use minimum number of reversible gates.
- Use minimum number of garbage outputs.
- Use minimum constant inputs.

II. BASIC DEFINITION OF REVERSIBLE LOGIC

A. Reversible logic Function:

A Reversible gate is a k-input, k-output circuit that produces a unique output pattern for each possible input pattern. Reversible gates [5] are circuits in which the number of outputs is equal to the number of inputs and there is one to one correspondence between the vector of inputs and outputs, i.e., it can generate unique output vector from each input vector and vice versa.

Example : Let the input vector be $I_v$, output vector $O_v$ and they are defined as follows, $I_v = (I_1, I_1, I_1, I_1, I_1)$ and $O_v = (O_1, O_1, O_1, O_1, O_1)$. For each particular $i$, there exits the relationship $I_i \leftrightarrow O_i$ [13].

This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits. The reversible logic circuits must be constructed under two main constraints. They are

- Fan-out is not permitted.
- Loops or feedbacks are not permitted

B. Basic Reversible logic Gates

The important basic reversible logic gates are, Feynman gate [7] which is the only 2*2 reversible gate which is as shown in the figure.1a and it is used most popularly by the designers for fan-out purposes. There is also a double Feynman gate [8], Fredkin gate [9] and Toffoli gate [10], New Gate[11], Peres gate[12], all of which can be used to realize important combinational functions and all are 3*3 reversible gates and are as shown in the figure.1a to figure.1e. The figures also shows the switching functions for terminals.
In the present paper SCL gate (Six Correction Logic) is used for the required correction in the BCD addition. In a BCD adder, the correction logic which generates the $C_{out}$ is given by,

$$C_{out} = S_3S_2 + S_3S_1 + C_4$$

### III. A 4 * 4 DKFG REVERSIBLE GATE

A 4 * 4 reversible gate DKFG already had been proposed [14] shown in figure 2. In this gate the input vector is given by $I_V$ = (0, A, B, C) and the corresponding output vector is $O_V = (P, Q, R, S)$.

### The DKFG gate can implement the conventional Boolean functions. Realization of AND operation, XOR operation, NOT operation and XNOR operation and also COPY operation shown in figure 2a and 2b.

We can implement half-adder by using DKFG gate as shown in figure 2c.

There is a one-to-one mapping between inputs and outputs of SCL gate and it can be used to add 6 to the sum in order to correct it to get the correct BCD sum [15].
We can use DKFG gate as a full-adder as shown in figure 2d.

Figure 2d. Implementation of DKFG gate as a full-adder

IV. CONVENTIONAL CARRY SKIP BCD ADDER

A. Conventional Carry Skip Adder

The circuit is as shown in figure 3. It uses two four bit adders, carry skip logic circuit and a correction logic circuit. The carry skip BCD adder is faster than the above BCD adder as it skips the propagation of carry input if $Z=1$. The carry propagate input $Z = Z_0, Z_1, Z_2, Z_3$ is generated at the output of a 4-input AND gate where $Z_0 = (A_0 \oplus B_0)$, $Z_1 = (A_1 \oplus B_1)$, $Z_2 = (A_2 \oplus B_2)$ and $Z_3 = (A_3 \oplus B_3)$. When $Z=1$, the carry input $C_{in}$ is propagated to reach $C_{out}$, otherwise it is skipped without propagating through the full adders. If $Z=0$, $C_4$ is propagated to $C_{out}$. Also whenever $C_{out} = 1$, correction logic adds six to the sum to generate the correct BCD sum as per rules of BCD addition.

At first we have used four DKFG reversible gates as a full adder to add two four bits BCD numbers $A_3 A_2 A_1 A_0$ and $B_3 B_2 B_1 B_0$. For initial input carry $C_{in}$ is used. And we got $C_4, S_3, S_2, S_1$, and $\Sigma S_0$. We have used three PERES gate for getting $Z = Z_0, Z_1, Z_2, Z_3$ where $Z_0 = (A_0 \oplus B_0)$, $Z_1 = (A_1 \oplus B_1)$, $Z_2 = (A_2 \oplus B_2)$ and $Z_3 = (A_3 \oplus B_3)$. An another PERES gate is used to create $P = Z C_{in} + C_4$. Then the SCL gate is used for six correction logic and from where we get the carry output $C_{out} = P \cdot C_{in} + C_4$. Another PERES gate is used for adding $S_1$ and $C_{out}$. Finally we get $\Sigma S_1$ and the generated carry is forwarded to next DKFG gate. Again the DKFG gate is used as a full adder to add the previous generated carry from the PERES gate, $S_3$ and $C_{out}$. And from this DKFG gate we get the $C_{out}$ and $\Sigma S_2$ and the generated carry is forwarded to the FG gate. Finally we get $\Sigma S_3$ from FG gate. Lastly we get the correct BCD sum as $\Sigma S_3 \Sigma S_2 \Sigma S_1 \Sigma S_0$.

In this paper we have designed 4-bit carry skip BCD adder shown in figure 4 using 4x4 DKFG reversible gate.

V. DESIGN OF CARRY SKIP BCD ADDER USING DKFG REVERSIBLE GATES

Figure 3. Carry Skip BCD Adder

Figure 4. Carry Skip BCD Adder using DKFG reversible gates
TABLE I

<table>
<thead>
<tr>
<th>Carry Skip BCD adder circuit</th>
<th>I. Different parameters</th>
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<tr>
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<td>No. of Garbage output</td>
<td>No. of Constant input</td>
<td>No. of reversible gates</td>
<td>Quantum cost</td>
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<td>15</td>
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VI. CONCLUSION

We have designed 4-Bit Carry Skip BCD Adder using DKG, PERES, SCL_FG reversible Logic gates and made a comparison in TABLE1. It gives the comparison of the different designs in terms of the important design parameters like the number of reversible gates, number of garbage outputs, and the number of constant inputs and the quantum cost. From the table it is seen that the present proposal uses the least number of gates producing the least number of garbage outputs and has the minimum quantum cost compared to other design methods. Using this circuit we can also construct 8bit, 16 bit and N bit Carry skip BCD adder in future

REFERENCES