A Novel and Efficient Mixed Signal VLSI Circuit for Multimode Demodulator

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Abstract— In this research paper, we proposed a mixed signal quadrature demodulator. This is integrated on embedded multi gigabit modem in 90 nm CMOS technology. Quadrature VCO is used to obtain the specified frequency range. IF PLL is designed to lock VQCO at specified frequency. Here a 3 bit ADC is used to obtain the high speed. To save power and area, unnecessary building blocks of ADC are excluded. Automatic gain control (AGC) is implemented to avoid clipping distortion experienced by the baseband ADCs. The results obtained in this project are used to satisfy the stringent power requirements of a mixed signal demodulator specifically for multi gigabit applications. The demodulator is integrated with IQ mixers, VQCO, Frequency synthesizers and baseband AGC. This demonstrates the maximum throughput at minimum power budget and highest level of integration. Baseband modem incorporates a mixed signal timing recovery loop to sample the symbols at optimum SNR based on Gardner timing error detector.

Keywords—90nm, ADC, AGC, mixed signal, low power, modem, multi gigabit

I. INTRODUCTION

CMOS wireless communication transceivers in the mm-wave regime, which offers several GHz of bandwidth [1-3]. Such systems generally require both low-power broadband demodulator and high-speed ADCs for portable multi-gigabit applications. For example, systems such as orthogonal frequency-division multiplexing (OFDM) and multi-input multi-output (MIMO) consume unreasonably high power due to the high resolution analog-to-digital converters (ADC) and complex signal processing. Hence, this is unsuitable for the high-speed mobile applications. In contrast, the single carrier modulation and direct-sequence spread spectrum (DSSS) are suitable for low resolution ADCs and digital signal processing to recover the multi-gigabit data signal, operating at hundreds or even thousands of the power consumption. There are tremendous potentials for such mixed-signal demodulator in the wireless consumer electronic market. The proposed circuits are implemented in 90nm CMOS and can be easily integrated with any mm-wave front-ends.

II. DESCRIPTION OF THE METHODS

A. Modulation Scheme

The required performance of a wireless receiver is determined by the intrinsic and extrinsic noise sources. Typically, the extrinsic sources include TX noise n RX band, inter modulation distortion, quantization noise, and imperfectly filtered interference. The noise figure (NF) of a receiver is normally determined by the low-noise amplifier (LNA) following the on-chip antenna in any radio environment. A millimeter-wave 90 nm CMOS receiver front-end, consisted of a LNA, mixer, and frequency synthesizer.

The receiver minimum sensitivity, related to this information, can be expressed as

\[ P_{\text{min}} = 10 \log(kT\cdot BW) + NF + LM + SNR_{\text{min}} \]

Where is K the Boltzmann constant, T is the absolute temperature in Kelvin, BW is the bandwidth occupied by the RF signal, NF is the noise figure of the receiver, LM is the link margin, and SNR_min is the minimum signal-to-noise ratio (SNR) required for the chosen modulation. To achieve a specific level of reliability in terms of bit-error rate (BER), the baseband SNR required for a suitable modulation scheme can be calculated as

\[ \text{SNR}_{\text{ADC}} = P_{\text{in}} - 10 \log(kT\cdot BW) - NF \]

Where \( P_{\text{in}} \) is the received input power level. A raw BER before error correction of 1E-06 is typically desirable for wireless communication systems.

The proposed non-coherent demodulator first synchronizes the ADC sampling clock to the middle of baseband symbols by incorporating a timing-recovery loop. When the baseband SNR is optimized, the DSP differentially demodulates DBPSK by complex multiplication.
B. Receiver Architecture

The quadrature demodulator is implemented to down convert a modulated IF carrier at 13 GHz to baseband using double-balanced passive mixers. The LO is generated by the quadrature voltage-controlled oscillator (QVCO) integrated with a frequency synthesizer. Baseband variable-gain amplifiers (VGA) are implemented with automatic gain control (AGC) and DC-offset compensation. The analog signal processor (ASP) reuses the power detector circuit within the AGC loop to detect the OOK signal. To extend sampling rate aggressively, the ADC is time-interleaved and implemented with 14 parallel comparators in each channel. The digitized signals are then fed to a digital baseband modem, performing either BPSK or DBPSK demodulation operation using mixed-signal synchronization architectures. This project presents the first fully integrated quadrature receiver with embedded analog and digital signal processors in deep-submicron CMOS technology.

C. Circuit Implementation

1) Frequency Synthesizer

The IF PLL is used to lock the QVCO to a frequency of 13GHz. This PLL features an integer-N type-II, fourth-order architecture. The first 2 cascaded divide-by-2 frequency dividers are implemented using current-mode logic (CML) topology. The remaining lower frequency dividers are implemented as true single-phase clock (TSPC) counters, featuring a division ratio of 120. The clock to the ADC and DSP is generated from a baseband clock synthesizer comprising a three-stage ring oscillator and features a third-order type-II baseband integer PLL. Different data rates (432MHz, 864MHz, 1.485GHz and 1.728GHz) are also available by programmable division ratio.

2) IQ Mixers

The input to the quadrature demodulator is a modulated IF carrier and is down converted to the baseband frequency. Conventional mixer pays the penalty for low conversion gain in a standard 1-V supply, consequently poor linearity. Therefore, the proposed double-balanced passive mixer utilizes a passive mixing core of RF transistors followed by a differential output buffer to compensate the conversion loss due to the passive mixing. The mixer provides a conversion gain of 3 dB with a bandwidth greater than 4 GHz and has a power consumption of 3 mW.

3) Quadrature Voltage Controlled Oscillator

The IF phase-locked loop (PLL) is designed to lock the free-running QVCO to 13 GHz. This frequency synthesizer features an integer-N, type-II, fourth-order architecture with a division ratio of 480. The varactor diodes and inductor form a LC-tank resonator. The mechanism of the parallel cross-coupled pairs forces two differential outputs to be 90 degrees out of phase. The output buffer of the QVCO is a source-follower stage and provides a differential voltage amplitude of 840 mV peak-to-peak with a 3-dB bandwidth of 24 GHz at a current consumption of 2.4 mA. The free-running QVCO exhibits a tuning range from 12 to 14 GHz and has a phase noise of 95 dB Hz at 1 MHz offset. The total power consumption is 15Mw.
4) VGAs with AGC and DC Offset Compensation

The baseband VGAs in each I and Q path are implemented with AGC and DC offset compensation loops. Each of the quadrature signal paths consists of three cascaded amplifiers to provide a maximum gain of 24 dB with a continuous gain variation of 27 dB. A DC offset compensation feedback loop is required to minimize this offset. It is achieved by connecting the differential output of the third VGA in opposite polarity to the differential output of the first VGA in a low-frequency feedback loop. To avoid clipping distortion to the baseband ADCs, AGC is required to keep the output power of the VGAs constant. It can be realized using a power detector, a differential-to-single-ended amplifier, a low-pass filter, and an op-amp. The output power of the VGA can be digitally controlled and set to a desired value through a 6-bit current-steering DAC.

5) Power Detector and On-Off Keying

The power detector circuit serves two purposes: to detect the output power from the VGAs and demodulate an OOK-modulated signal. It consists of two double-balanced Gilbert-cell mixers with a common differential load. Each Gilbert-cell mixer performs the squaring function by connecting the gates of the upper-stack and lower-stack transistors to the same input signal. The output of the power detector is the summation result of squared quadrature signals (I^2+Q^2). Total power consumption is 7.5 mW.

6) High-Speed Analog to Digital Converter

The ADC performs ultra-low-power processing by removing track-and-hold amplifier. First, seven comparators sample the data and compare with its own voltage reference to generate the output in thermometer code. Next, the outputs are converted to gray code and then to binary code. The entire operation requires only a single-phase clock and is also time-interleaved to achieve a high conversion rate at a low-power budget.
In this circuit, the input is first compared with a voltage reference, $V_{\text{ref}}$ using the differential pair M1-M2. The comparison result is then transferred to the output latch by current mirrors M3-M5 and M4-M6. When clk is low, M9 is off and the latch senses the decision of $V_{\text{in}}$ and $V_{\text{ref}}$. In this phase, when $V_{\text{in}} > V_{\text{ref}}$, Im1 is greater than Im2, thus decreasing the voltage at $V_{\text{out}}$. Then, at the output node, the drain current of quickly charges up the negative impedance cross-coupled pairs and brings the output node voltage close to (or $\text{GND}$ when $V_{\text{in}} < V_{\text{ref}}$). On the other hand, when clk goes high, M9 is turned on to short the outputs to equal value and speeds up regeneration. The overload recovery time is determined by M9, the output parasitic capacitance and the transconductance of M7-M8.

7) Mixed signal back end

The 3-bit time-interleaved ADC in each channel produces a total of 6 bits (3 bits on rising edge and 3 bits on falling edge of the baseband clock) to the digital modem. The positively and negatively latched bits are denoted by subscripts A and B, respectively. The digital modem consists of a mode select block, coherent DSP demodulator, bit synchronization, and non-coherent DSP demodulator.

8) Digital Modem

Using the sampled baseband signal, a low-power mixed-signal symbol timing-recovery loop is designed for reliable data detection in modern digital communications system. In the operation of timing-recovery loop, the baseband frequency synthesizer loop is disabled because the bit synchronizer shares part of the baseband VCO loop. Its implementation is based on a 3-bit Gardner timing-error detector (GTED) without using any digital multiplication.
The Gardner loop method is developed for BPSK and QPSK symbol synchronization. It basically detects the zero crossing point of the symbols, and corrects the gradient using neighboring sample values. The recursion process is performed to reduce the error for timing recovery, and a timing tone is recovered though convergence. To avoid the interpolation operation needed to estimate the correct sampling instance, a 4-bit digital timing-error signal is converted to analog domain using a 5-bit high-speed current-steering DAC. Then, the timing-error signal is filtered by a passive loop filter at a loop bandwidth of 2 MHz. This error signal controls the phase of the baseband VCO. The digital timing-error detector block is capable of handling high data rate at low power consumption; it does not require any digital multiplier and utilizes 657 gates (2163 m) to perform a 6-bit input error calculation.

III. RESULTS

Fig. 12 VCO output 1 with amplitude 2.27 Volts and time period 0.1 microseconds (LC tank based)

Fig. 13 VCO output 3 with amplitude 2.3 Volts and time period 0.1 microseconds (LC tank based)

Fig. 14 VCO output amplitude 3.4 Volts and time period 15 nanoseconds

Fig 15 Transient response of 3 bit flash ADC

Fig 16 transient response of 3 bit flash ADC
IV. CONCLUSION

A mixed-signal broadband quadrature receiver with an embedded modem, which leverages unique boundaries between analog and digital circuits to realize a high-performance IC design with compact area and low-power dissipation. A high-speed digital ASIC chip integrated with analog front-end is successfully demonstrated and performs desired multi-gigabit demodulation operations. The proposed architecture presents a fully integrated system that simultaneously achieves multi-gigabit modem functionality and maintains the overall power budget in sub-Watt regions. The mixed-signal demodulator can perform a multi-gigabit BPSK demodulation up to 3.5 Gb/s data rate. The mixed-signal demodulator can perform multi-gigabit OOK and DBPSK demodulations. This demonstrates for the first time a unique multi-gigabit solution for low-power applications.

In future we can implement the above system with 45 nm technology. By doing so we can obtain 10-15% area reduction, up to 60% power reduction, superior quality of service, concurrent design and fine of analysis. Also by using the clock gating concept in quadrature VCO, area overhead can be further reduced.

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