Design of Serial in Serial out And Serial In Parallel out Shift Register Using Double Edge Triggered D Flip Flop

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Abstract—Using low power Double Edge Triggered D-Flip flop that paper specify the design of Serial In Serial Out (SISO), Serial In Parallel Out (SIPO) shift register. Double Edge Triggered Flip Flops are bistable flip-flop circuits in which data is latched at rising and falling edge of the clock signal. Using Double Edge Triggered D-Flip flop using NMOS transistor permits the data processing rate to be preserved while using lower clock frequency. Therefore, power consumption in DETFF based circuits can be reduced. And design shift register (siso, sipo) using double edge triggered d flip flop.

Keywords-- DETFF, delay, PDP, shift registers.

I. INTRODUCTION

The conventional D – Flip flop is the very basic design of DFF. Latches are often called level-sensitive because their output follows their inputs as long as they are enabled. They are transparent during this entire time when the enable signal is asserted. There are situations when it is more useful to have the output change only at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. Thus, we can have all changes synchronized to the rising or falling edge of the clockry.

Access to the internal memory is controlled by the clock input. The memory element reads its data input value when instructed by the clock and stores that value in its memory. The output reflects the stored value, probably after some delay. In CMOS circuits the memory is formed in two ways. The most popular synchronous digital circuits are edge-triggered flip-flops. D-type flip-flop (DFF) is one of the most fundamental building block in modern VLSI systems and it contributes a significant part of the total power dissipation of the system. This paper is organized as follows Section II & III explains the basics of DETFF and shift registers. The nominal simulations are discussed in Section IV.

II. DOUBLE EDGE TRIGGERED D-FLIP FLOP

The most common approach for improving the performance is to increase the clock frequency. However, use of high clock frequency has a number of disadvantages.

Power consumption of the clock system dramatically increases and clock uncertainties take significant part of the clock cycle. Other problems include degradation of the clock waveform due to the non-ideal clock distribution, power supply noise and cross-talk. An alternative clocking strategy relies on the use of storage elements capable of capturing data on both clock edges (rising and falling edge). In this case, the same data throughput can be achieved with half of the clock frequency. In other words double edge clocking can be used to save half of the power on the clock distribution capitalized.

Figure 1: DETFF [1]

Figure 1: DEFFT [1]
The Double edge triggered flip-flop shown in Fig 1 has less average power and lowest PDP than conventional designs.

### Comparative Result

<table>
<thead>
<tr>
<th>Flip Flop’s</th>
<th>Average Power (µW)</th>
<th>Delay (µs)</th>
<th>PDP (aJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DETFF [1]</td>
<td>3.25</td>
<td>3.72</td>
<td>12.09</td>
</tr>
<tr>
<td>PROPOSED DETFF</td>
<td>2.75</td>
<td>3.10</td>
<td>10.23</td>
</tr>
</tbody>
</table>

### Table 2

<table>
<thead>
<tr>
<th>Flip Flop’s</th>
<th>Average Power (µW)</th>
<th>Delay (µs)</th>
<th>PDP (aJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DETFF [1]</td>
<td>1.509</td>
<td>10.72</td>
<td>16.17</td>
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<td>DETFF [2]</td>
<td>7.45</td>
<td>11.09</td>
<td>82.63</td>
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<tr>
<td>PROPOSED DETFF</td>
<td>4.5</td>
<td>3.49</td>
<td>15.705</td>
</tr>
</tbody>
</table>

III. **Shift Registers**

In digital circuits, Shift register is a group of flip-flops used to shift or transfer data from flip-flop to flip-flop. It’s a group of D flip-flops connected in a chain and the clock of the flip-flops is connected in a synchronous manner.

Shift register has 2 basic functions such as; data storage and data movement. Shift register has 4 classifications namely; Serial In Serial Out (SISO), Serial In Parallel Out (SIPO), Parallel In Serial Out (PISO) and Parallel In Parallel Out (PIPO). A Serial In Serial Out (SISO) Shift Register The Serial In Serial Out (SISO) shift register accepts data serially (one bit at a time on a single line). It produces the stored information on its output also in serial form. And the basic Serial In Serial Out (SISO) shift register is shifted the bit in serial.so output will be get in serial.

The data string is given at input and is shifted right one stage each time 'Data Advance' is brought high. At each advance, the bit on the far left (i.e. 'Din') is shifted into the first flip-flop's output. The bit on the far right (i.e. 'Dout') is shifted out and lost. The data are stored after each flip-flop on the 'Q' output, so there are four storage 'slots' available in this arrangement; hence it is a 4-bit register. To give an idea of the shifting pattern, imagine that the register holds 0000 (so all storage slots are empty). As 'Data In' presents 1, 0,1,1,0,0,0,0 (in that order, with a pulse at 'Data Advance' each time, this is called clocking or strobing to the register, this is the result. The left hand column corresponds to the left-most flip-flop's output pin, and so on. So the serial output of the entire register is 10110000. This arrangement is the hardware equivalent of a queue.

B. Serial In Parallel Out (SIPO) Shift Register

This configuration allows conversion from serial to parallel format. Data input is given serially, as described in the SISO section above. Once the data are stored, each bit appears on its respective output line and all bits are available simultaneously.
IV. SIMULATION RESULTS

Figure 3: SIPO shift register

Figure 4: Waveform Between Voltage And Time For Delay.

Figure 5: Output Of Serial In Serial Out Shift Register using DETFF

Figure 6: Output Of Serial In Parallel Out Shift Register Using DETFF
V. CONCLUSION

In this paper, we have designed a high performance Double Edge Triggered D-Flip Flop based shift register (siso,sipo). We have simulated double edge triggered D flip flop for exploring the average power, delay and PDP. The Simulation result showing doule edge triggered d flip flop is suitable for low power application.

REFERENCES


About Author

Ms. Namrata Rapartiwar is M.Tech scholar from Gyan Ganga Institute of Technology and Sciences in embedded system and VLSI design subject.

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