Abstract—This paper presents an active clamp is added in multioutput fly-back converter to achieve soft switching (Zero voltage switching). The selected fly-back topology operated in Continuous Conduction mode. Fly-back converter provides multiple output which are lower and higher voltages than input voltage. When the converter operates at hard switching there will be more switching losses, and there is also a transformer leakage inductance which results in voltage stress on main switch. To overcome this disadvantage an active clamp circuit is incorporated in to multioutput fly-back converter. With the help of active clamp circuit, the transformer leakage energy is recycled, and zero-voltage-switching (ZVS) for primary main switch is achieved.

Keywords—Multioutput fly-back converter, active clamp circuit, continuous conduction mode, leakage inductance, ZVS(zero voltage switching

I. INTRODUCTION

Power supplies are the most popular part of electronic test equipment. It is a device that supplies electric power to an electrical load. Power supplies are used extensively in industrial application to meet the following purposes:

(a) Isolation between the source and load; (b) Reduction of size and weight; (c) Controlled direction of power flow; (d) High conversion efficiency; (e) Input and output waveform with a low total harmonic distortion for small filters; (f) Controlled power factor if the source is an ac voltage.

To achieve these specifications switched-mode power supply are selected. These supplies include high frequency converter topologies to get improved performance and to realize in compact size, [1]. A fly-back converter switching power supply topology is widely used in application below 100W. Compare to other topologies in [1],[2], fly-back is simple, less components and low cost. They are especially popular in multi-output application, due to the low parts count one diode and capacitor per output. In a fly-back converter, when more than one output is present, the output voltages track the input voltage and the load, far better than they do in the forward converter.

This is because of the absence of the output inductor, so the output capacitor connects directly to the secondary of the transformer and acts as a voltage source during the turned off period of the switch. So it is essential to design these supplies using high frequency converter topologies to get improved performance compact size, reduce the switching losses [3],[4]. The switch in the fly-back converter is operated at hard switching. Therefore the voltage and current stress of switch suffered from the transformer leakage inductance is very high and also an EMI problem from the hard switching limit the power rating for higher power application [5],[6]. To overcome these drawbacks, and to achieve ZVS, active clamp circuit is added. Active clamping is an effective means to clamp the voltages across semiconductor devices as well as to achieve soft switching [7]-[9]. The active-clamp circuit provides the benefits of recycling the transformer leakage energy while minimizing turn-off voltage stress across the power switch [10]-[11]. In addition, the active-clamp circuit provides a means of achieving zero-voltage-switching (ZVS) for the power switch and subsequent lowering of the output rectifier di/dt. This results in decreased rectifier switching loss and output switching noise. The analysis, design and implementation of a 70W active clamp fly-back converter is presented in this paper to achieve zero voltage switching (ZVS) for main switch. With the auxiliary switch, clamp capacitor and resonant inductor, the surge energy stored at the leakage inductance can be recycled by the active clamp circuit.

II. SYSTEM ANALYSIS

Fig.1 shows the block diagram of multioutput fly-back converter and Fig 2 shows circuit configuration of the active clamp fly-back converter. The magnetizing inductance is represented as Lm. The resonant inductance \( L_r \) is the sum of transformer leakage inductance and external inductance. The resonant capacitance \( C_r \) is equal to the parallel combination of the parasitic capacitance of main switch S1 and auxiliary switch S2.
The auxiliary switch S2 and clamp capacitor $C_{\text{clamp}}$ represent the active clamp circuit to recycle absorb the surge energy due to the leakage inductance so as to reduce the voltage stress of S1. The resonant capacitance $C_r$ and inductance $L_r$ are resonant to achieve ZVS operation for main switch, S1.

Before the system analysis some assumptions are made as:

1) The resonant period generated by the clamp capacitance $C_{\text{clamp}}$ and resonant inductance $L_r$ is greater than turn off time of main switch;
2) The resonant inductance is less than magnetizing inductance ($L_r < L_m$);
3) All semiconductors (switches and diodes) are ideal;
4) the converter is operated in the continuous conduction mode;
5) the energy stored in the resonant inductance is greater than energy stored in the resonant capacitance in order to achieve ZVS operation for main switch.

Fig 1. Block diagram of multioutput flyback converter

Fig 2. Circuit of active clamp flyback converter

Fig 3. Equivalent circuits for each interval
Fig 4. waveform of active clamp flyback converter

Fig 3 and Fig 4 shows necessary equivalent circuits for each interval and waveforms respectively. During interval T0-T1: At T0, switch S1 is on, and the auxiliary switch, S2, is off. The output rectifier, D1, is reversed biased. The magnetizing inductance is being linearly charged as it charges "normal" fly-back operation. T1-T2: S1 is turned off at T1. Cr is charged by the magnetizing current which is also equal to the current through the resonant inductor. The charge time is very brief, leading to an approximately linear charging characteristic. In interval T2-T3: At T2, Cr is charged to the point where the anti-parallel diode of S2 starts to conduct. The clamp capacitor fixes the voltage across resonant inductor Lr and the transformer magnetizing inductance to Vc (=NVout), forming a voltage divider between the two inductances,(where Vc is clamp voltage, N is turns ratio and Vout is output voltage).Since Cclamp is much larger than resonant capacitor Cr, nearly all of the magnetizing current is diverted through the diode to charge the clamp capacitor. Consequently, the voltage appearing across the magnetizing inductance, Vpri, decreases as Vc increases, according to the voltage divider action, Vpri=Vc(Lm/Lr+Lm). In interval T3-T4: At T3, primary voltage Vpri has decreased to the point where the secondary transformer voltage is sufficient to forward bias D1. The transformer primary voltage is then clamped at Vin+ NVout by the output capacitance to approximately NVout. Lr and Cclamp begin to resonate. In order for S2 to achieve ZVS, the device should be turned on before clamp capacitor current icclamp reverses direction.

During interval T4-T5: The auxiliary switch, S2, is turned off at T4, effectively removing Cclamp from the circuit. A new resonant network is formed between the resonant inductor and the MOSFET parasitic capacitances. The transformer primary voltage remains clamped at NVout as Cr is discharged. In interval T5-T6: Assuming the energy stored in Lr is greater than the energy stored in Cr, At T5 Cr will be sufficiently discharged to allow S1’s body diode to start conducting. The voltage across the resonant inductor becomes clamped at Vin + NVout. During interval T6-T7: S1 is on, and the secondary current is decreasing as the resonant inductor current increases. At T7, the secondary current decreases to zero (because the resonant inductor current has equal the magnetizing current), and D1 reverse biases, allowing the polarity to reverse on the transformer primary. The magnetizing and resonant inductances begin to linearly charge again, starting another switching cycle.

III. DESIGN PROCEDURE

Assumed that the maximum duty cycle of active clamp fly-back converter is Dmax. The turn ratio between the transformer primary side and secondary side is equal to

\[ N = \frac{N_1}{N_2} = \frac{V_{in, min} D_{max}}{V_o (1 - D_{max})} \]  

(1)

If the clamp capacitance is large enough, the voltage across resonant inductor is neglected.

- Magnetizing inductance,

\[ L_m = \frac{\eta [V_{in, min} T_{sw}]^2}{2 P_o (min) T_{sw}} \]  

(2)

- Peak current of the main switch

\[ I_{s, main, peak} = \frac{P_o}{\eta V_{in, min} D_{max}} + \frac{V_{in, min}}{L_m} D_{max} T_{sw} \]  

(3)

- Voltage stress of rectifier diode

\[ V_{D_o, max} = \frac{V_{in, max}}{N} + V_o \]  

(4)

- Peak secondary diode current

\[ I_{D_o, peak} = \frac{2 P_o}{V_o (1 - D_{max})} \]  

(5)

- Output capacitance is given by,

\[ C_o = \frac{D_{max} P_o}{f_{sw} V_o \Delta V_c} \]  

(6)
\[ V_{\text{out ripple}} = 1\% \text{ of } V_o, \]

- Resonant capacitance : \( C_r = \text{parallel combination of the parasitic capacitance of main switch } S_{\text{main}} \text{ and auxiliary switch } S_{\text{aux}}. \)

- Resonant inductor \( L_r \) is given by,
\[
L_r = \frac{1}{4\pi^2 f_r^2 C_r} \quad \text{................(7)}
\]

- Clamp capacitance is given by,
\[
\frac{\left[1 - D_{\text{min}} V_{\text{in}}\right] T_{\text{sw}}}{\pi^2 L_r} \quad \text{................(8)}
\]

where \( D_{\text{min}} V_{\text{in}} = (D_{\text{max}} V_{\text{in min}})/V_{\text{max min}} \)

**IV. EXPERIMENTAL RESULT**

A proposed converter for 70W is designed and simulation circuit of multioutput active clamp fly-back converter is shown in Fig 5. Table 1 and 2 gives simulation and hardware results respectively. Fig 6 and Fig 7 shows the experimental waveforms of the gate-to-source voltages of main switch and auxiliary switch of main switch. The time delay between the auxiliary switch turn-off and main switch turn-on to ensure main switch turn on at ZVS respectively. Fig.8 gives the experimental waveforms of gate signals of main switch \( V_{s1,gs} \) and auxiliary switch \( V_{s2,gs} \) and transformer primary voltage \( V_{p1, ipri} \). When main switch is turned on, the transformer primary side voltage is equal to \( V_{\text{in}} \). If the main switch is turned off, the primary side voltage equals \(-N V_{\text{out}}\). Fig. 9 shows the gate-to-source and drain- to source voltage for main switch. Before the mains switch is turned on the drain-to-source voltage has been reached zero. Fig. 10 gives the switch \( V_{s1,gs} \) and auxiliary switch \( V_{s2,gs} \). and transformer experimental waveform of clamp capacitor voltage.

**TABLE I. SIMULATION RESULT**

<table>
<thead>
<tr>
<th>Required output(V)</th>
<th>( V_{o1} )</th>
<th>( V_{o2} )</th>
<th>( V_{o3} )</th>
<th>( V_{o4} )</th>
<th>( V_{o5} )</th>
<th>( V_{o6} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Obtained output Voltage(V) for full load</td>
<td>12.8</td>
<td>409</td>
<td>310</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Obtained output Voltage(V) for no load</td>
<td>21</td>
<td>563</td>
<td>432</td>
<td>23</td>
<td>23</td>
<td>23</td>
</tr>
</tbody>
</table>

**Fig 5. Simulation circuit**

**Fig 6. The gate-to-source voltages of main switch(blue) in channel 1 and gate to source voltage of auxiliary switch(green) in channel 3. when the main switch is ON the auxiliary switch will be OFF, both switches will not be on simultaneously.**
Fig 7. This figure shows the time delay between the auxiliary switch (green in channel 3) when it turns-off and main switch (blue in channel 1) turns-on to ensure main switch turn on at Zero voltage Switching.

Fig 8. The gate-to-source voltages of main switch (blue) in channel 1 and gate to source voltage of auxiliary switch (green) in channel 3. And the transformer primary voltage $V_{pri}$ (red) in channel 2 and primary current $I_{pri}$ (pink) in channel 4.

Fig 9. The gate-to-source voltage (blue) of main switch, gate to source voltage of auxiliary switch (green) and drain-to-source voltage (red) of main switch. Before the mains switch is turned on the drain-to-source voltage of main switch has been reached zero.

Fig 10. $V_{clamp}$ voltage $V_{clamp}$ (red) in channel 2 along with main switch (blue) and auxiliary switch (green) gate voltages in channel 1 and 2 respectively.

TABLE II.

<table>
<thead>
<tr>
<th></th>
<th>Vo1</th>
<th>Vo2</th>
<th>Vo3</th>
<th>Vo4</th>
<th>Vo5</th>
<th>Vo6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required output(V)</td>
<td>6.3</td>
<td>400</td>
<td>300</td>
<td>15</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>Obtained output Voltage(V) for full load</td>
<td>6.4</td>
<td>368</td>
<td>283</td>
<td>14.2</td>
<td>14.2</td>
<td>14.2</td>
</tr>
<tr>
<td>Obtained output Voltage(V) for no load</td>
<td>6.5</td>
<td>573</td>
<td>440</td>
<td>14.6</td>
<td>14.6</td>
<td>14.6</td>
</tr>
</tbody>
</table>

V. CONCLUSION

The operation of 70W active clamp flyback converter for multioutput is analysed. The proposed converter is designed and tested and the required multioutput output voltages are obtained. The transformer leakage energy is recycled and ZVS for switch is achieved and voltage stress on switch is reduced.

REFERENCES


[10] Analysis, design and implementation of an active clamp flyback converter 2005 IEEE.