Low-Power and Low-Area Dual Dynamic Node Hybrid Flip-Flop Featuring Efficient Embedded Logic for Low Power CMOS VLSI Circuits Using 120nm Technology

Meghana Pelleti¹, T. Krishna Murthy², K. Neelima³

¹PG Scholar, ²,³Assistant Professor, Dept. of ECE, Sree Vidyanikethan Engineering College, Tirupathi

Abstract— In this paper, a new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFF-ELM) based on DDFF are introduced. The DDFF offers power and area reduction when compared to the conventional flip-flops. The main aim of DDFF-ELM is to reduce pipeline overhead which arises due to the pipeline setup time, propagation delay and clock skew. It gives an area, power and speed efficient method to incorporate complex logic functions into the flip-flop. The performance comparisons are made in 120nm technology by using Digital Schematic and Microwind. And also here, DDFF and DDFF-ELM are compared with other flip-flop designs by implementing a 4-b Johnson Counter. Here the performance improvements indicate that proposed designs are well suited for modern high performance designs.

Keywords—Flip-flops, high-speed, low-power, embedded logic, leakage power, DDFF, pipeline overhead.

I. INTRODUCTION

Technology is moving forward from low scale integration to large scale and VLSI. The speed is also increasing from megahertz (MHz) to gigahertz (GHz). With the continuous advancing process of technology and speed of operation, the system requirements are also rising up. In deep-pipelined architectures, pushing the speed additional up demands a lower pipeline overhead. This overhead is the latency related to the pipeline elements, like the flip-flops and latches. Intensive work has been dedicated to improve the performance of the flip-flops within the past few decades. Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal.

After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes.

Among all the types of flip-flops and latches, mostly D Flip-flop latches are used. They are often called as level-sensitive because their output follows their inputs as long as they are enabled. They are transparent during this entire time when the enable signal is asserted. There are situations when it is more useful to have the output change only at the rising or falling edge of the enable signal, which is usually the controlling clock signal.

In this paper, different types of flip-flop architectures are compared. They are Power PC 603, Hybrid Latch Flip-flop (HLFF), Semi-dynamic Flip-flop (SDFF), Conditional Data Mapping Flip-flop (CDMFF), and Cross Charge Control Flip-flop (XCFF). In general HLFF and SDFF are classic high performance flip-flops. They are having hybrid architecture, that has combined advantages of both dynamic and static structures. In addition, SDFF has a capability of incorporating logic very efficiently, because unlike the true single phase latch (TSPC), only one transistor is driven by the data input. This helps in reducing the pipeline overhead. All these flip-flops are aiming at reduction of power, delay and area. The disadvantages in the above flip-flops are reduced in DDFF and DDFF-ELM.

A recent paper introduced, in which a flip-flop architecture named Cross Charge Control Flip-flop (XCFF), which has advantages over SDFF and HLFF in terms of both power and speed. There are some disadvantages in XCFF like large hold-time requirement, redundant power dissipation, large power consumption and susceptibility to charge sharing at the internal dynamic nodes.

In this paper, we introduce a new Dual Dynamic Node Hybrid Flip-Flop (DDFF) and a novel embedded logic module (DDFF-ELM). Both DDFF and DDFF-ELM eliminate the drawbacks of XCFF. These are free from unwanted transitions resulting when the data input is stable at zero. DDFF-ELM provides a speed, area, and power efficient method to reduce the pipeline overhead.
The performance of modern high performance flip-flops are compared with that of DDFF.

The remaining paper is divided as follows. Here Section II describes different types of flip-flop architectures and disadvantages of the existing flip-flop architectures and challenges in achieving high performance. In Section III, the proposed DDFF architecture and its operation, design and working principle are provided. Section IV details the proposed ELM. Finally in Section V, we conclude with the results and improvements of the proposed flip-flop designs over the existing modern high performance designs.

II. ANALYSIS OF DIFFERENT TYPES OF FLIP-FLOP ARCHITECTURES

The flip-flop designs are basically grouped as static and dynamic design styles. The master-slave designs include, transmission gate based master-slave flip-flop and the Power PC 603 master-slave latch. Power PC 603 (Figure. 1) is one of the most efficient classic static structures. The advantages of Power PC include low-power keeper structure and low latency direct path. The keeper structure in the circuit saves the leakage power. Latency is the time to complete a single instruction from start to finish. The large D-Q delay resulting from the positive setup-time is one of the disadvantages of this design. The large data and CLK node capacitances make the design inferior in performance. Despite among all these cons, static designs still remain as low power solution when the speed is not considered as a primary concern.

The dynamic flip-flops includes the modern high performance flip-flops. They are divided into purely dynamic designs and pseudo-dynamic structures. The distinctive performance improvements are achieved by having an internal precharge structure and a static output. They are called as the semi-dynamic or hybrid structures because of having a dynamic frontend and a static output. HLFF (Figure.2) and SDFF (Figure.3) fall under this category. Here the CLK overlaps to perform the latching operation.

Here Power PC means Performance Optimization With Enhanced RISC Performance Computing. They dissipate comparatively low power and they are also having low clock-to-output (CLK-Q) delay. In synchronous systems, the latching elements have the delay overhead which is expressed by the data-to-output (D-Q) delay rather than CLK-Q delay. Here, D-Q delay is the combination of CLK-Q delay and the setup-time of the flip-flop. But the static designs lack the low D-Q delay due to their large positive setup-time, and also most of them are susceptible to flow through resulting from CLK overlap.

HLFF is not the fastest but has a lower power consumption when compared to SDFF because of the longer stack of nMOS transistors at the output node makes it slower than SDFF and causes large hold-time requirement. Due to this large hold time requirement, makes the integration of HLFF to complex circuits difficult process. And also HLFF is inefficient in embedding the logic.
Figure 3. Semi-Dynamic Flip-Flop (SDFF).

SDFF is the fastest classic hybrid structure, but it has high power consumption because of the large CLK load as well as the large precharge capacitance. Its speed is high when compared to that of the HLFF.

In conventional semi-dynamic designs, the major sources of power dissipation are the redundant data transitions and large precharge capacitance. The Conditional Data Mapping Flip-Flop (CDMFF) which is present in Figure. 4, is the most efficient attempt to reduce the redundant data transitions in the flip-flop.

Figure 4. Conditional Data Mapping Flip-Flop (CDMFF).

CDMFF uses an output feedback structure to conditionally feed the data to the flip-flop which reduces overall power dissipation by eliminating unwanted transitions when a redundant event is predicted. Considerable speed performance is there, since there are no added transistors at the output node, similar to that of the HLFF.

The presence of the conditional structures in the critical path increase the hold time requirement and D-Q delay of the flip-flop. The CDMFF circuit is bulky and cause an increase in power dissipation at higher data activities due to the additional transistors added for the conditional circuitry.

In a wide variety of designs, the large precharge capacitance results due both the output pull-up and the pull-down transistors are driven by the precharge node. Most of the capacitance at this precharge node is due to the transistors being driving large output loads. This drawback is considered in the design of XCF (Figure. 5).

Figure 5. Cross Charge Control Flip-Flop (XCF).

XCF reduces the power dissipation by splitting the dynamic node into two, each one separately driving the output pull-up and pull-down transistors. The total power consumption is almost reduced without any degradation in speed because, only one of the two dynamic nodes is switched during one clock cycle. XCF has a comparatively lower CLK driving load. The major drawback of this design is that, the redundant precharge at node X2 and X1 for data patterns containing more 0s and 1s respectively. Due to the conditional shutoff mechanism, the large hold time requirement appears, and a low to high transition in the CLK when the data is low, causes charge sharing at node X1. This charge sharing can trigger erroneous transition at the output, unless the inverter pair INV1-2 is carefully skewed. The problem of charge sharing becomes very high when complex functions are embedded into the design.

III. PROPOSED DDFF ARCHITECTURE

In Dual Dynamic Node Hybrid Flip-Flop (DDFF), there are two nodes in the circuit among which one is purely dynamic and another is pseudo-dynamic.
So, called as dual dynamic. As it is having dynamic front end and static output, it is hybrid in nature. So this is the reason for calling this flip-flop as DDFF (Figure. 6).

In DDFF, node X1 is pseudo-dynamic with a weak inverter acting as a keeper. Node X2 is purely dynamic when compared to XCFF. Here we provide unconditional shutoff mechanism at the frontend where as conditional shutoff mechanism in XCFF. The DDFF operates in two phases:
1) The Evaluation Phase, when CLK is high, and
2) The Precharge Phase, when CLK is low.

The actual latching occurs in evaluation phase during 1-1 overlap of CLK and CLKB. If D is high (prior to this overlap period), node X1 is discharged from NM0-2, this switches the cross coupled inverter pair INV1-2 which causes node X1B to high and output QB discharge through NM4. For low level, node X1 retained by inverter pair INV1-2, for the rest of evaluation phase no latching occurs. Node X2 is held high throughout evaluation period by pMOS transistor PM1. As CLK falls low, the circuit enters in the precharge phase and node X1 pulled high through PM0, switching the state of INV1-2. During this period node X2 is not actively driven by any transistor, it stores the charge dynamically. The outputs at node QB and maintain their voltage levels through INV3-4. If D is low i.e zero (prior to the overlap period), node X1 remains high and node X2 pulled low through NM3 as the CLK goes high. Thus, node QB is charged high through PM2 and NM4 is held off. At the end of the evaluation phase, as the CLK falls low, node X1 remains high and X2 stores the charge dynamically.

The circuit exhibits negative setup time due to the short transparency period defined by the 1-1 overlap of CLK and CLKB allows the data to be sampled even after the rising edge of the CLK before CLKB falls low. The minimum time period before the CLK edge is setup time and the minimum time period after the CLK edge is the hold time, where the data should be stable so that proper sampling is possible. Here setup time and hold time depend on the CLK overlap period.

IV. PROPOSED ELM

As earlier we mentioned, the major advantage of the SDFF is the capability to incorporate the complex logic functions efficiently. The efficiency in terms of speed and area can be predicted from the fact that an N-input function can be realized in appositive edge triggered structure using a pull-down network (PDN) consisting of N transistors as shown in Figure. 7.

This embedded structure offers a very fast and small implementation. Although SDFF is capable of offering efficiency in terms of speed and area, it is not a good solution as far as power consumption is concerned. So we consider SDFF with embedded logic for comparative purposes.

The proposed dual dynamic node hybrid flip-flop with logic embedding capability (DDFF-ELM) is shown in Figure. 8.
In the proposed model, the transistor driven by the data input is replaced by the PDN and the clocking scheme in the frontend is changed. The reason for this in clocking is the charge sharing, which becomes uncontrollable as the number of nMOS transistors in the stack increases. The same reason makes XCFF also incapable of embedding complex logic functions. As the size and number of the stacked nMOS transistor increases, the charge sharing becomes uncontrollably large.

Here by using the above flip-flops a Johnson up-down counter can be designed and the results are compared accordingly.

From the above Figures. 9, 10, and 11, Johnson Counter is designed with the help of SDFF, XCFF and DDFF respectively. All the results are compared with respect to counter.

V. RESULTS

The performance comparisons of the all flip-flops are given in the below table.

<table>
<thead>
<tr>
<th>Flip-Flop</th>
<th>No. of Transistors</th>
<th>Memory used (%)</th>
<th>Area (µm²)</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power PC 603</td>
<td>20</td>
<td>11.1</td>
<td>393.2</td>
<td>0.300mW</td>
</tr>
<tr>
<td>HLFF</td>
<td>20</td>
<td>10.6</td>
<td>710.6</td>
<td>0.206mW</td>
</tr>
<tr>
<td>SDFF</td>
<td>23</td>
<td>12.0</td>
<td>478.2</td>
<td>0.210mW</td>
</tr>
<tr>
<td>CDMFF</td>
<td>22</td>
<td>12.2</td>
<td>454.9</td>
<td>0.202mW</td>
</tr>
<tr>
<td>XCFF</td>
<td>21</td>
<td>10.2</td>
<td>367.6</td>
<td>51.626µW</td>
</tr>
<tr>
<td>DDFF</td>
<td>18</td>
<td>9.5</td>
<td>305.1</td>
<td>18.084µW</td>
</tr>
<tr>
<td>DDFF-ELM</td>
<td>23</td>
<td>8.4</td>
<td>287.3</td>
<td>16.531µW</td>
</tr>
<tr>
<td>SDFF-ELM</td>
<td>22</td>
<td>8.8</td>
<td>316.4</td>
<td>73.442µW</td>
</tr>
</tbody>
</table>

From the above table we can notice that, the performance of power and area are increased in DDFF and also DDFF-ELM when compared to the other types of flip-flops. The graphical representation of the results for the DDFF are given in the below figure.12.
From the above results, we can notice the performance improvements in DDFF and DDFF-ELM.

By using these flip-flops, as earlier mentioned, Johnson Counter is designed. The performance comparisons for these counters are given below in Table II.

### Table II

<table>
<thead>
<tr>
<th>Flip-Flop</th>
<th>No. of Transistors</th>
<th>Memory Used (%)</th>
<th>Area (µm²)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDFF</td>
<td>92</td>
<td>33.5</td>
<td>1378.3</td>
<td>0.542</td>
</tr>
<tr>
<td>XCFF</td>
<td>84</td>
<td>30.5</td>
<td>1200.9</td>
<td>0.114</td>
</tr>
<tr>
<td>DDFF</td>
<td>72</td>
<td>27.7</td>
<td>1034.5</td>
<td>0.104</td>
</tr>
</tbody>
</table>

From the above table, we can notice that the power and area are reduced in DDFF when compared to the other flip-flops.

VI. CONCLUSION

In this paper, a new low power and low area DDFF and a novel DDFF-ELM were proposed. The proposed DDFF eliminates the redundant power dissipation present in XCFF. Comparison of the proposed flip-flop with the other flip-flops showed that it exhibits lower power dissipation along with area and speed performances. The efficiency of the flip-flop and the ELM were further highlighted using Johnson up-down counter. It was proven that the proposed architectures are well suited for modern high performance designs where area, delay overhead and power dissipations are of major concern.

REFERENCES


