Digital RF Memory Based Target simulator For Radar.

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Abstract— Idea of Radar target simulator is to electronically generate the Radar illuminated environment without switching on actual Radar transmitter in the field. These Radar target simulators are used to develop, optimize and test the Radar System Design and Algorithms in the Lab. Conventional testing method has its own limitations. In this paper DRFM based target simulator is presented which overcome the conventional method limitations.

Keywords— DRFM Digital Radio Frequency Memory, FPGA Field Programmable Gate Array, SSB Single Sideband, DDS Direct Digital Synthesis.

I. INTRODUCTION

The functionality of short range Radar is detecting the range and velocity. To Test the capability of Radar system, the field trails are normally carried out in the remote places and these trails are includes lot of efforts and results into lot of expenditure. We cannot test the performance of the system in all the possible scenarios.

Instead an alternate test setup may be designed, which will simulate the real scenario and evaluate the short range Radar performance in different scenarios and with the results we can do the any modification of Hardware or software such that it fulfils all the required functions in all the test conditions. This simulation reduces the testing phase of system development, and all the possible scenarios we can study the system response, which otherwise not possible in real world.

II. RADAR TESTING USING CONVENTIONAL METHOD

The conventional method for testing the RADAR System is shown in fig 1. The main Functionality of any primary RADAR System is to detect the target range based upon the delay between transmitted pulse and received pulse and target velocity, based upon the Doppler shift between transmitted frequency and received frequency.

In this method range is simulated using delay lines and target velocity is simulated using signal generator and RF mixer.

Fig 1: RADAR System testing using conventional method.

The conventional method is having its own advantages and disadvantages.

The merit of conventional method is simple.

The demerits of conventional method are:

As the range (i.e. Delay) is added the loss will increase so we need to add amplifiers in between in order to maintain the minimum signal level.

Quadrature null effect: It is the problem of adding Doppler by DSB-Sc method where both positive and negative Doppler signals are added. But in the real scenario, either positive or negative frequency will exist so we have to add the Doppler using SSB modulation.

III. DRFM ARCHITECTURE

DRFM is the significant block in RADAR Simulators. The basic idea of the DRFM can be found in reference [1]. A basic block diagram of DRFM system is shown in Fig.2 [1]. The modern application example for RADAR simulator found in reference [2]. The Basic Functionality of DRFM technique is to down convert the incoming RF Signal (Normally in GHz) to an Intermediate Frequency (IF Normally in MHz) and the sampled at Higher sampling rate that satisfy the Nyquists Theorem. Then store the digitized signal in High Speed Memory.
The Memory modules adds the delay and Doppler for simulate the target Range and velocity. The digital Signal is reconstructed by DAC and then Up-converted back to RF frequency using the same Local Oscillator which has been used for down-conversion of the input RF signal.

In simple terms the DRFM Memories maintains the coherency of the incoming signal and modifies the phase of the signal to simulate any target.

![Fig 2. Block diagram of DRFM system.](image)

**IV. DRFM BASED DYNAMIC TARGET SIMULATOR**

The demerits of conventional method are overcome by using DRFM based target simulator. It contains ADC, DAC and a memory module which is implemented by FPGA. The incoming RADAR pulse is modified in the FPGA in phase and spectrum to simulate the required target.

![Fig 3. Functional block DRFM Based RADAR Target Simulator.](image)

The FPGA consists of a vast array of configurable logic tiles, multipliers, and memory resources. This technology provides the signal-processing engineer with the ability to construct a custom data path that is tailored to the application at hand.

The delay and Doppler blocks are implemented on Xilinx System generator. The delay block is implemented using shift registers and FIFO modules. The delay is the value in steps of 8.3nsec is the delay that need to added between the input and output. For high values of delay FIFO modules are used for low value of delay shift registers are used.
The Doppler block is implemented using DDS. A digitally-controlled method of generating multiple frequencies from a reference frequency source has evolved called Direct Digital Synthesis (DDS).

Here Xilinx Virtex-4 SX FPGA is used so it is specified in that token and the clock speed is 120MHz is also given in that token. The yellow tokens are In and Out tokens that convert the floating point data into fixed point and vice-versa. Since all the logic implementation in FPGA is fixed point so MATLABs floating point values need to be converted into fixed point.

V. RESULTS

a. Delay addition

The above figure shows the addition of delay between the input and output. The top Pulse is the input pulse and the bottom pulse is the DRFM output pulse.

\[ \text{Range} = \frac{CT}{2} \]

\( T \) – Time delay between transmission and receiving pulse. To simulate a target of range 1 mt we need to add a delay of 6.67 ns between the transmitted pulse and receiving pulse.
b. Doppler Addition

The required Doppler is generated using DDS, then it is multiplied with the incoming pulses. The above figure shows the video signal of RADAR sensor which having a frequency as well as time shift i.e., velocity and range simulation.

Doppler frequency \( (F_d) = \frac{2 \times V_r \times \lambda \times \cos \theta }{\lambda} \)

Where \( \lambda \) – wave length and \( \theta \)– angle between target and radar.

C. Graphical User Interface.

The required target parameters are set using this GUI. The major parameters that are set are target range, velocity and its strength.
VI. CONCLUSION

The Dynamic DRFM Based Target Simulator has been developed which overcome the limitations of conventional method limitations. The software coding in VHDL is done for generating a Target with various range and velocities. The Primary target detection capability under various test conditions has been evaluated.

REFERENCES


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