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A comparative analysis for 3 and 5-Level Inverter for Diode Clamped Topology with Harmonic analysis

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***Abstract*— A Multilevel Power Converter structure is based on the concept of High power and medium voltage situations. Its concept is to use a series of power semiconductor switches with several layer voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Multilevel converter operates both in inverter and rectifier mode in a power electronic circuit. So, we are focusing on multilevel inverter. Multilevel inverters (MLI) have become more popular over the years in electric high power application with the promise of less disturbances and the possibility to function at lower switching frequencies than ordinary two level inverters. This paper represents information about Diode Clamped Inverter topology for different level, such as for three level and five level. Simulation results are given to better understand the advantages.**

***Keywords*—Two Level Inverter, Multilevel Power converters (MLPC).**

I. Introduction

Some medium voltage motor drives and utility application require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to convert only one power semiconductor switch directly. A multilevel power converter structure has been introduced as an alternatives in high power and medium voltage situation. A multilevel converter not only achieves high power rating but also enables the use of renewable energy resources.

The concept of a multilevel to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveforms. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however the rated voltage of the power semiconductor switches depends only the rating of the dc voltage sources to which they are connected.

A multilevel converter has several advantages over a conventional two level converter that uses high switching frequency pulse width modulation (PWM).1.*Stair case waveform quality* - Multilevel converter not only can generate the output voltages with very low distortion, but also to reduce the dv/dt stresses; therefore electromagnetic compatibility can be reduced.2.

Common mode (cm) voltage- Multilevel converters produce smaller CM voltage; therefore the stress in the bearings of a motor connected to a multilevel motor drive can be reduced.CM voltage can be advanced modulation strategies.3.Input current- Multilevel converters can draw input current with very low distortion.4.*Switching frequency* - Multilevel Converter can operate at both fundamental switching frequency and high switching frequency PWM .It is noted that lower switching frequency usually means lower switching loss and higher efficiency.

II. Types Of Multilevel Inverters

Instead of two level inverter in Multilevel Inverter,multilevel can be get from different Inverter topology. Source wise it is separate DC source and common DC source. Using separate DC source cascaded inverter is made and using common DC sources Flying capacitor inverter and Diode Clamped Inverters are made.

III. Different Topologies

- Neutral Point Clamped Multilevel Inverter
- Capacitor Clamped Multilevel Inverter
- Cascaded Multilevel Inverter
- Generalized Multilevel Inverter
- Reversing Voltage Multilevel Inverter
- Modular Multilevel Inverter
- Generalized Multilevel Current Source Inverter

A. Characteristics of different topologies of inverters

Diode clamped particularly the 3 level one, have taken interest in motor drive application as it needs only one common voltage source and many simple and efficient PWM algorithm have been developed though it has DC link capacitor voltage problem.

In case of 4-level diode clamped inverters there is limitation for the reason of reliability and complexity considering DC link balancing and more number of clamping diodes.

Flying capacitors inverters need more number of capacitors and also the capacitors are bulkier for higher voltage ratings which are critical problems on the sizing of the inverter.

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Cascaded inverters structurally don't have any problems of DC link voltage unbalancing or the requirement of the larger capacitors but requires many separated DC sources which is considered as a major advantage with the present day rechargeable batteries.

The batteries are rated for 12V/24V, in order to build an inverter system for high voltage, motor drive applications for critical loads, they are connected in series to obtain the higher voltage rating.

B. Salient features of multilevel inverters

Synthesis of higher voltage level using power devices of low voltage ratings.

Increased number of voltage levels which leads to better voltage waveforms and reduced total harmonic distortion in output voltage.

Reduced switching stresses on the devices due to the reduction of step voltages between the levels.

It solves harmonic and EMI problems, but also avoids possible high frequency switching stress dv/dt.

Low switching losses and better electromagnetic compatibility for high power applications.

C. Comparison of Conventional and Multilevel Inverter

TABLE I
COMPARISON OF DIFFERENT TOPOLOGY

Conventional Inverter	Multilevel Inverter
Higher THD in output voltage.	Low THD in output voltage.
More switching stress on devices	Reduced switching stress on devices
Not applicable for high voltage applications	Applicable for high voltage applications
Higher voltage levels are not produced	Higher voltage levels are produced
Since dv/dt is high, EMI is also high	Since dv/dt is low, EMI is also low
Higher switching frequency is used hence switching frequency losses is high	Lower switching frequency can be used and hence reduction in switching losses
Reliability is high	Reliability can be improved back swapping of levels is possible

IV. MULTILEVEL DIODE CLAMPED INVERTER

According to the Diode Clamped Multilevel Inverter, the number of levels can be increased by increasing the number of switches and the number of capacitors.

To limit the three levels, where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the DC bus, so the terminology neutral point clamped inverter is introduced. An even number of voltage levels, the neutral point is not accessible and the term multiple point clamped is sometimes applied. Due to the capacitor voltage balancing issues, the diode clamped inverter implementation has been mostly limited to the three level inverter.

Diode clamped inverter, in which the diode is used or the clamping device is used to clamp the DC voltage so as to achieve steps in the output voltage. An 'm' level diode clamped inverter typically consists of (m-1) capacitors on the DC bus and produces 'm' level of phase voltages and (2m-1) line voltages. An 'm' level inverter leg requires (m-1) capacitors, 2(m-1) switching devices and (m-1)(m-2) clamping diodes.

In this circuit the DC bus voltage is split into 3 levels by two series connected bulk capacitors, C_1' and C_2'. The middle point of the two capacitors 'n' can be defined as the neutral point. The output voltage V_{an} has three states: $V_{DC}/2$, 0, $-V_{DC}/2$.

For voltage level $V_{DC}/2$, switches S_1 and S_2 need to be turned on. For $-V_{DC}/2$, switches S_1' and S_2' need to be turned on and for the 0 level S_2 and S_1' need to turned on. The key components that distinguish this circuit from a conventional two level inverter are D_1 and D_1'. These two diodes clamp the switch voltage to half the level of the DC bus voltage. When both S_1 and S_2 turn on, the voltage across a and 0 is V_{DC}, i.e. $V_{ao}= V_{DC}$.

In this case, D_1' balances out the voltage sharing between S_1' and S_2' with S_1' blocking the voltage across C_1 and S_2' blocking the voltage across C_2'. The output voltage V_{an} is A.C and V_{ao} is DC. The difference between V_{an} and V_{ao} is the voltage across C_2, which is $V_{DC}/2$. If the output is removed out between 'a' and 'o', then the circuit becomes a DC/DC converter, which has three output voltage levels, $V_{DC}/2$, 0, $-V_{DC}/2$.

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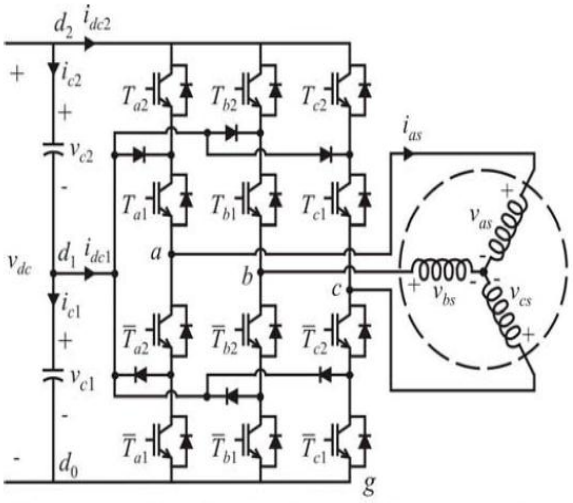

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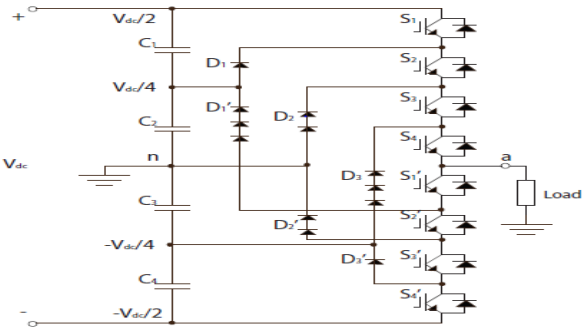

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Fig.1. Diode Clamped Multilevel Inverter. (a) 3-Level Inverter. (b) 5-Level Inverter.

TABLE II
COMPARISON BETWEEN 3-LEVEL AND 5-LEVEL DIODE CLAMPED INVERTER

Components	3-Level	5-Level
Power semiconductor switches	4	8
Clamping diodes per phase	2	12
DC bus capacitor	2	4

It have some advantages like all of the phases share a common DC bus, which minimize, the capacitance requirement of the converter. This reason, back to back is also practical used for high voltage back to back interconnection or adjustable speed drive. Efficiency is high for fundamental frequency switching.

Although it have some disadvantages like Real power flow is difficult for a single inverter between the intermediate DC levels will tend to overcharge or discharge without monitoring and control. The number of clamping diodes required is quadritically related to the number of levels which can be cumbersome for unite with a high number of levels.

Huge application can be seen in the area of STATCOM, FACTS devices and main thing is that it produces an interface between HVDC and HVAC transmission lines as well as serves as a variable speed drive for high power medium voltage (2.4 KV to 13.8 KV) motors.

A. Switching States of both topology

Case 1: 3-level Inverter

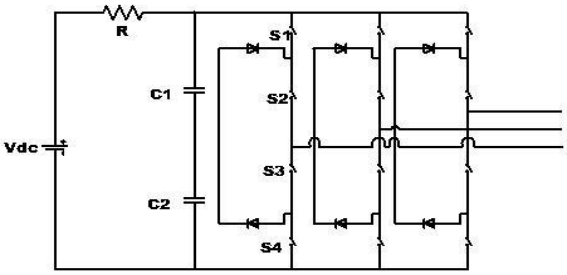

Fig. 2. 3-Phase,3-level Diode Clamped Inverter

Each phase node are connected to any node of the capacitor. Connections of the phase to junction can be accomplished by switches S1 and S2 both on and off respectively. Connections are accomplished by switching sequence S1 on and S2 off. In this representation, S1 and S2 are on for the positive half cycle. S3 and S4 are on for the negative half cycle. For 0 level, S2 and S3 should be on. With the switching state, the phase current will flow into the junction through diode D1 if it is negative or out of the junction through diode D2 if the current is positive.

Table III.
Switching State of Diode Clamped

Sl. No.	Switching State	Output Voltage
1.	S1 = ON, S2 = ON	$+V_{DC}$
2.	S2 = ON, S3 = ON	0
3.	S3 = ON, S4 = ON	$- V_{DC}$

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Case 2: 5-level Inverter

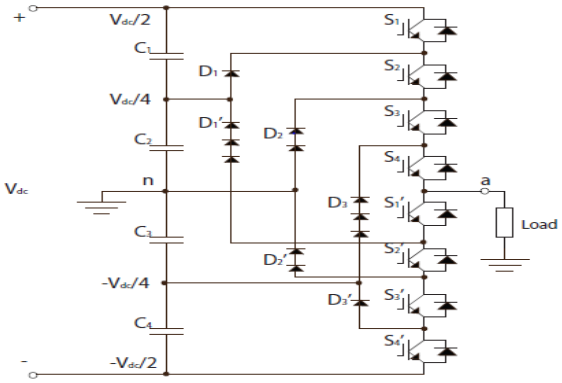


Fig.3. 5-level Diode Clamped Inverter

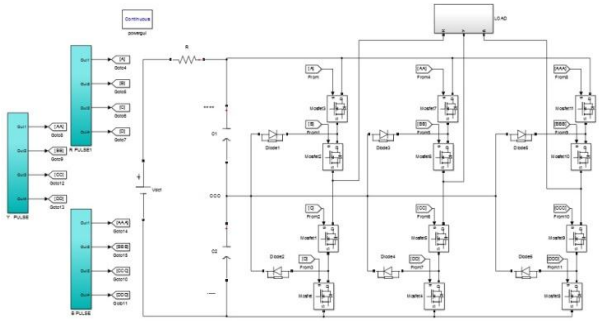
For the voltage $V_{DC}/2$, all the upper switches are turned on, connecting point a, to the $V_{DC}/2$ potential. For the output voltage $V_{DC}/4$ switches S_2, S_3, S_4 and S_1' are turned on and the voltage is held by the help of the surrounding clamping diodes D_1 and D_1'. For the voltage levels $-V_{DC}/4$ or $-V_{DC}/2$ clamping diodes D_2 and D_2' or D_3 and D_3' hold the voltage. For the voltages $V_{DC}/2$, the current, when both voltage and current are positive, goes through the four top or bottom switches. For the other states positive current, while voltage is positive, goes through the D_x diodes and negative current through the D_x' diodes and also the switches in between the clamping diodes and the load.

Table IV.
Switching State of 5-level Diode clamped

S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	**Output voltage**
1	1	1	1	0	0	0	0	$V_{DC}/2$
0	1	1	1	1	0	0	0	$V_{DC}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{DC}/4$
0	0	0	0	1	1	1	1	$-V_{DC}/2$

V. Simulation Result

The three level inverter with RL load, consists of voltage source inverter which is used to produce the staircase voltage. Three level PWM concept is based on the constant carrier frequency which is used to reduce the harmonic contents in the output voltage and decrease the voltage rating of the power devices. [9-10]For the verification of the proposed multilevel inverters, it is simulated using MATLAB/SIMULINK. It helps for the confirmation of PWM reduction switching strategies. For both type of multilevel inverter input DC Voltage kept constant at V_{dc} =100V and 10 ohm resistance and 0.01 Henry inductance taken as load, modulation index used here 0.8, switching frequency at 10 KHz.



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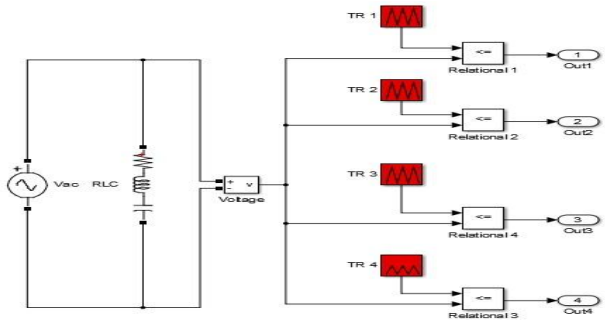

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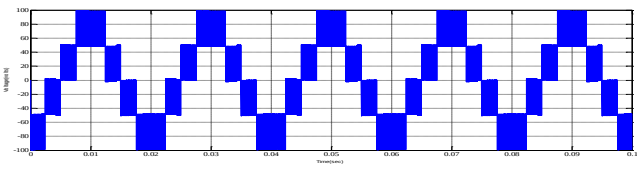

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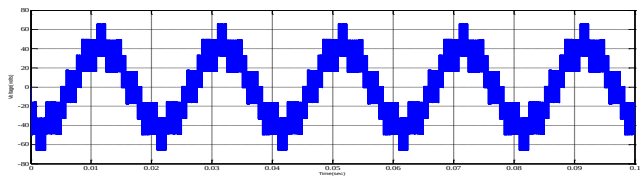

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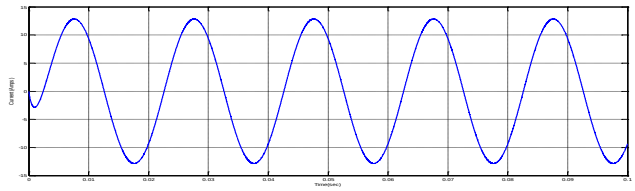

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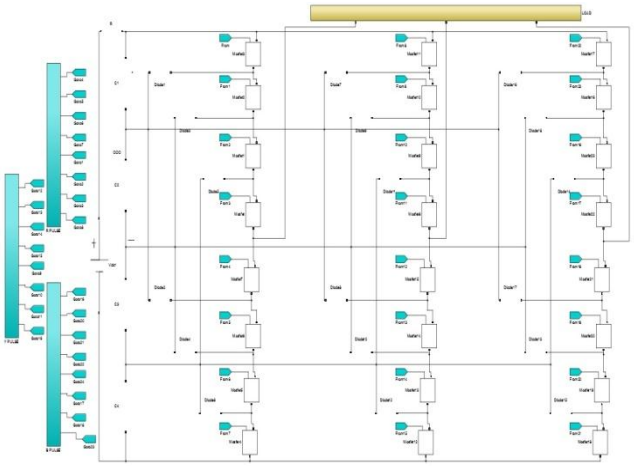
Fig.4. 3-Level Diode clamped Inverter (a) Simulated Diagram (b) Diagram in the Subsystem (c) Output Line Voltage (d) Output Phase Voltage (e) Output Current Wave Form.



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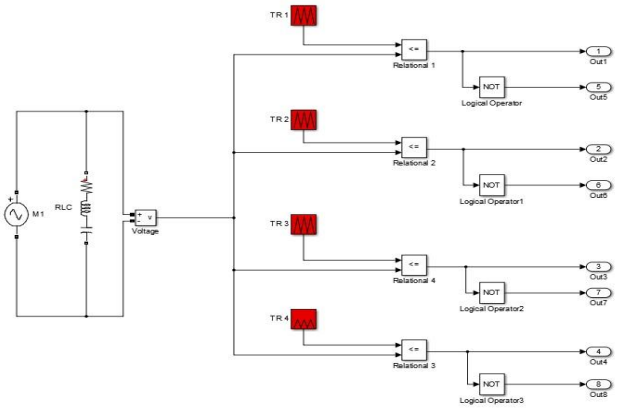

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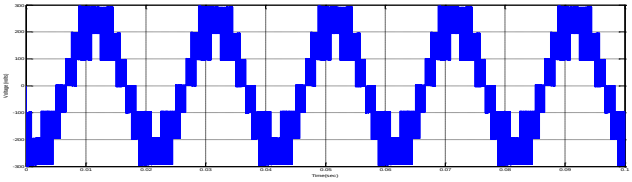

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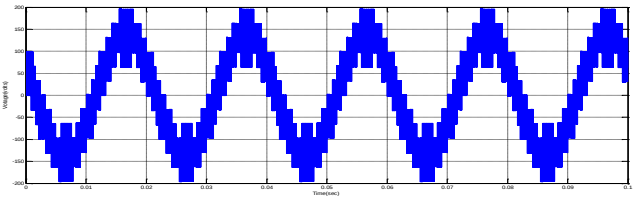

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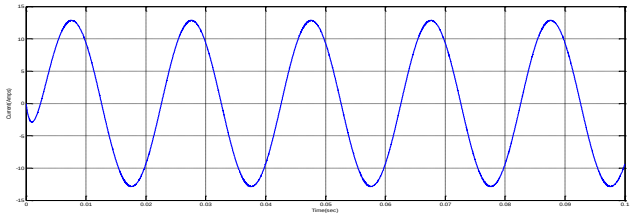

(e)

Fig. 5. 5-Level Diode Clamped Inverter (a) Simulation Diagram, (b) Diagram in the Subsystem, (c) Line Voltage, (d) Phase Voltage, (e) Current Waveform.

In fig. 4.(a) simulation diagram of three phase three level inverter which have done in matlab is shown. To give gate pulses there a subsystem is created which has shown in fig.4(b).Here pulses have generated by comparing between sine wave and four carrier wave.Simulated results are shown in fig.4.(c),(d),(e) as a line voltage, phase voltage and current wave form.

Five level three phase multilevel inverter simulated diagram shown in fig.5(a) and pulses are generated by four carrier comparision with sine wave which is shown in fig.5(b) and simulated result are shown in fig.5(c),(d),(e) as a line voltage, phase voltage and current wave form for five level three phase inverter.

Three level and Five level diode clamped multilevel inverter has been simulated and analyzed and in the table V. practical output value is given.

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Table V.
Simulated output of 3-level multilevel inverter

Type of Topology	Pole Voltage	Line Voltage	Phase Voltage	Current Harmonics
For Three Phase Three Level				
Diode Clamped	50, 0, -50	99.6, 49.8, 0.1, -49.5, -99.7	66.3, 49.7, 33.1, 16.7, 0, -15.8, -33, -49.1, 65.8	0.46%
For Three Phase Five Level				
Diode Clamped	–	49.5, 40.6, 29.95, 21.7, 12.3, 0, -12.3, -21.7 , -29.95, -40.6, 0-49.5	72.3, 47.1, 23.9, 0, -23.9, -47.1, -72.3	0.66%

VI. HARMONICS ANALYSIS

The steady state distortion to voltage and current waveforms due to non-linear electric loads. The frequent cause of power equality problems in power grid are harmonic frequencies. For low and medium power applications, square wave or quasi-square wave form voltage but for high power application sinusoidal waveform with low distortion are required. Harmonics content present in the output of a DC to AC inverter can be eliminated either by using a filter circuit or by employing PWM techniques. Use of filter has disadvantages of large size and cost, whereas PWM technique reduces the filter requirement to the minimum or to zero depending on the type of application.

In power switching inverter, one of the most modulation technique is SPWM technique. In order to generate gate signals, sinusoidal reference voltage waveform as compared with the triangular voltage waveform. The fundamental frequency control method is done to minimize the switching losses. This technique is used for elimination of harmful low-order harmonics in the multilevel inverter. To compare the harmonics performance of the symmetrical and asymmetrical technique. Total Harmonics Distortion (THD) is done. The THD is one which evaluates the quantity of harmonics contents in the output waveform and is modular index performance for power converters.

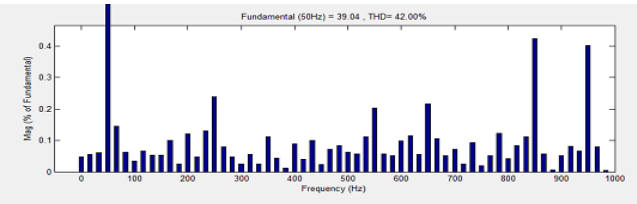

Figure 6. THD of 3-level Diode Clamped MLI

The three level Diode Clamped Multilevel Inverter is simulated and the result is analysed to determine the THD. By applying FFT, the THD of the output voltage waveform is determined to be 42.00%.

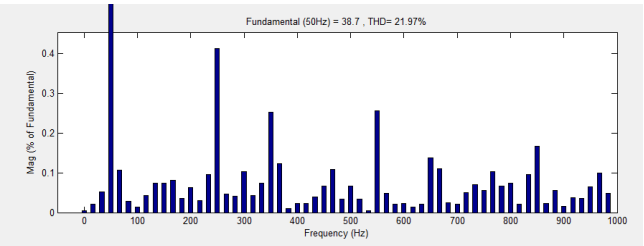

Fig.7. THD od 5-level Diode Clamped

The five-level diode clamped multilevel inverter is simulated and the result is analyzed to determine the THD. By applying FFT, the THD of the output voltage waveform is determined to be 21.97%.

VII. CONCLUSION

Diode Clamped Inverter Topology, of a three-level inverter have been simulated using "Sine Pulse Width Modulation Technique". With increase of level THD of output waveform as well as filtering problem decreases .The theoretical results were validated by simulations. It is found that the voltage harmonics reduces on increasing the levels but the current harmonics increases. The modular multilevel converter offers superior technical characteristics for HVDC, especially without passive filters at the AC side and DC side. Voltage sharing of the devices will be handled automatically by the topology. The waveform shape will lead to sinusoidal waveform due to which THD will be reduced and the harmonics as well. Numerical solutions of sub-module with higher number of switching require considerable time.

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