International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 5, Issue 11, November 2015)

An Improved Clock Gating Method Flip-Flop Using Auto Gated Style

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Abstract: **Power Dissipation plays an important role as development of transportable devices as concern. therefore during this paper we have a tendency to discuss regarding reduction of Dynamic power and Static power consumption in Flip-Flops, as a result of flip-flops square measure the key power consumption components attributable to increase of speed. The novel approach we have a tendency to square measure aiming to style the circuit supported look ahead clock gating that is to be used for the temporal arrangement constraints for every clock pulses. The facultative clock pulses for the derived temporal arrangement signals to the gated logic that is to be saves the ability from the flip-flops. we have a tendency to use each clock gating and power gating to cut back the overall power consumption of circuts. These results square measure calculated exploitation TSMC018 technology by exploitation Tanner Tools**

Keywords: **Clock Gating, Power Gating, Tanner Tools**

I. INTRODUCTION

Energy dissipation could be a terribly crucial parameter that must be taken under consideration throughout the look of VLSI circuits. With the speedy progress in semiconductor technology, chip density and operation frequency have exaggerated, creating the ability consumption in battery-operated transportable devices a serious concern. High power consumption reduces the battery service life. The goal of low-power style for powered devices is so to increase the battery service life whereas meeting performance necessities.

Reducing power dissipation could be a style goal even for non-portable devices since excessive power dissipation leads to exaggerated packaging and cooling prices moreover as potential dependability issues.

To address these problems directly, it's essential to grasp the various sorts and the CMOS technology is that it's presently the foremost dominant digital IC implementation technology. Power dissipation in CMOS digital circuits is classified into 2 types: peak power and time-averaged power consumption. Peak power could be a dependability issue that determines each the chip time period and performance.

The free fall effects, caused by the excessive fast current owing through the resistive power network, have an effect on the performance of a style attributable to the exaggerated gate and interconnect delay.

This huge power consumption causes the device to overheat that reduces the dependability and lifelong of the circuit. conjointly noise margins square measure reduced, increasing the possibility of chip failure attributable to disturbance. CMOS digital circuits occur in 2 forms: dynamic and static. Dynamic power dissipation happens within the logic gates that square measure within the method of switch from one state to a different. throughout this method, any internal and external capacitance related to the gate's transistors must be charged, thereby overwhelming power. Static power dissipation is related to inactive logic gates (i.e., not presently switch from one state to another). Dynamic power is vital throughout traditional operation, particularly at high operational frequencies, whereas static power is a lot of vital throughout standby, particularly for powered devices

For dynamic loss reduction we have a tendency to square measure exploitation Clock Gating technique and for static loss reduction we have a tendency to square measure suing RTPG technique explained below.

II. CLOCK GATING AND POWER GATING

Clock gating could be a common technique utilized in several synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding a lot of logic to a circuit to prune the clock tree. Pruning the clock disables parts of the electronic equipment in order that the flip-flops in them don't have to be compelled to switch states. switch states consumes power. once not being switched, the switch power consumption goes to zero, and solely leak currents square measure incurred.[1]

Clock gating works by taking the modify conditions connected to registers, and uses them to gate the clocks. thus it's imperative that a style should contain these modify conditions so as to use and get pleasure from clock gating.

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This clock gating method may also save vital die space moreover as power, since it removes massive numbers of muxes and replaces them with clock gating logic. This clock gating logic is mostly within the type of "Integrated clock gating" (ICG) cells. However, note that the clock gating logic can amendment the clock tree structure, since the clock gating logic can sit within the clock tree.

Power gating could be a technique utilized in microcircuit style to cut back power consumption, by motility off this to blocks of the circuit that aren't in use. Additionally to reducing stand-by or leak power, power gating has the advantage of facultative Iddq testing.

III. Integrated Clock And Power Gating

Clock Gating and Power Gating square measure 2 most typically used style strategies to avoid wasting dynamic and leak power severally. however regarding desegregation the 2 solutions such they complement every other? during this post, i'll point out an easy thanks to do therefore.

IV. Clock Gating

Clock signals square measure present in synchronous circuits. The clock signal is employed during a majority of the circuit blocks, and since it switches each cycle, it's Associate in Nursing activity issue of one. Consequently, the clock network lands up overwhelming an enormous fraction of the on-chip dynamic power. Clock gating has been heavily utilized in reducing the ability consumption of the clock network by limiting its activity issue. basically, clock gating reduces the dynamic power dissipation by disconnecting the clock from Associate in Nursing unused circuit block.

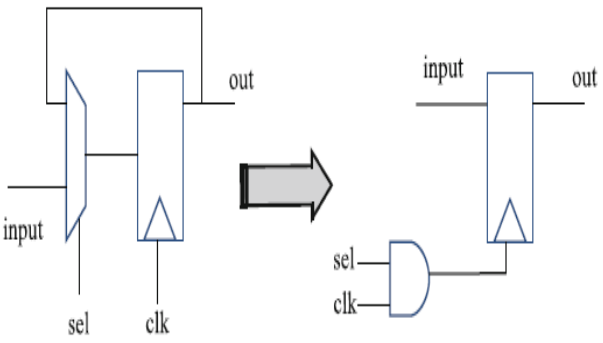

Fig1:Clock Gating

Fig. 2.1 In its simplest type, clock gating may be enforced by looking for the signal that determines whether or not the latch can have a brand new knowledge at the tip of the cycle. If not, the clock is disabled exploitation the signal

Traditionally, the system clock is connected to the clock pin on each flip-flop within the style. This leads to 3 major parts of power consumption:

1. Power consumed by combinatorial logic whose values square measure dynamical on every clock edge;
2. Power consumed by flip-flops – this contains a non-zero worth even though the inputs to the flip-flops square measure steady, and also the internal state of the flip-flops is constant;
3. Power consumed by the clock buffer tree within the style. Clock gating has the potential of reducing each the ability consumed by flip-flops and also the power consumed by the clock distribution network.

Clock gating works by distinguishing teams of flip-flops sharing a typical modify signal (which indicates that a brand new worth ought to be clocked into the flip-flops). This modify signal is ANDed with the clock to come up with the gated clock, that is fed to the clock ports of all of the flip-flops that had the common modify signal.

For superior style with short-clock cycle time, the clock skew can be vital and wishes to be taken into careful thought. a very important thought within the implementation of clock gating for ASIC designers is that the graininess of clock gating. Clock gating in its simplest type is shown in Fig. 2.1. At this level, it's comparatively simple to spot the modify logic. during a pipelined style, the result of clock gating may be increased. If the inputs to at least one pipeline stage stay a similar, then all the later pipeline stages may also be frozen.

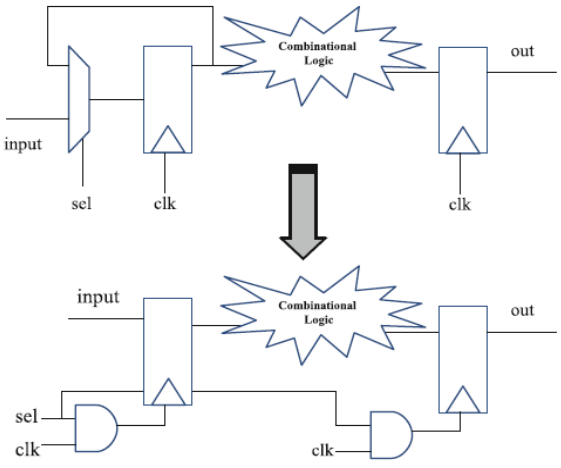

Fig.2: In pipelined styles, the effectiveness of clock gating may be increased. If the inputs to a pipeline stage stay a similar, then the clock to the later stages may also be frozen

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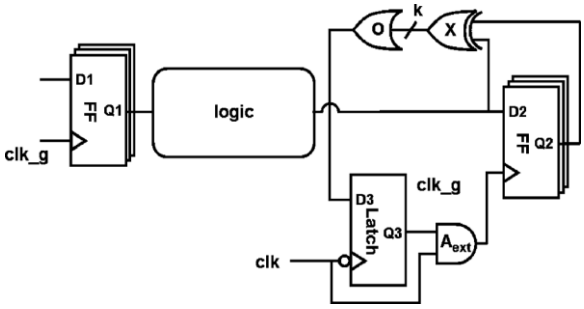
Figure 2 shows a similar clock gating logic being employed for gating multiple pipeline stages. this is often a multi-cycle improvement with multiple implementation tradeoffs, and might save vital power, usually reducing switch activity by 15–25%. except pipeline latches, clock gating is additionally used for reducing power consumption in dynamic logic. Dynamic CMOS logic is usually most popular over static CMOS for building high speed electronic equipment like execution units and address decoders. in contrast to static logic, dynamic logic uses a clock to implement the combinatory circuits.

Dynamic logic works in 2 phases, pre charge and judge. throughout pre charge (when the clock signal is low) the load capacitance is charged. throughout judge part (clock is high) counting on the inputs to the pull-down logic, the capacitance is discharged.

V. Data Driven Clock Gating Technique



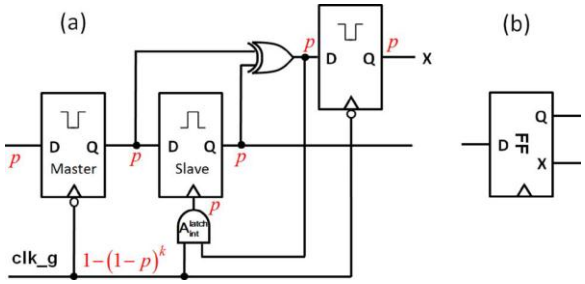
In knowledge Driven Clock gating technique gated clock signal was disabled whenever their was switch activity was tired the Input. The structure consists of logic gate that compares the input and output for each flip-flop and every one the outputs square measure tied to the logic gate so as to come up with a modify signal which can drive latch with logic gate clock gating circuit. Whenever the input was modified to Associate in Nursingy flip-flop then logic gate generates an modify signal and it passed on generates a clock modify signal to the grouping.

Data-driven gating is shown in on top of fig,A FF finds out that its clock may be disabled within the next cycle by XORing its output with this computer file which will seem at its output within the next cycle. The outputs of XOR gates square measure ORed to come up with a joint gating signal for FFs, that is then fast to avoid glitches. the mixture of a latch with logic gate is employed by business tools and is named Integrated Clock Gate (ICG) it's helpful to cluster FFs whose switch activities square measure extremely related .

Data-driven gating suffers from a awfully short time-window wherever the gating electronic equipment will properly work. this is often illustrated in Fig The accumulative delay of the XOR, OR, latch and also the AND gater should not exceed the setup time of the FF. Such constraints might exclude 5%-10% of the FFs read-only storage being gated attributable to their presence on temporal arrangement crucial methods.

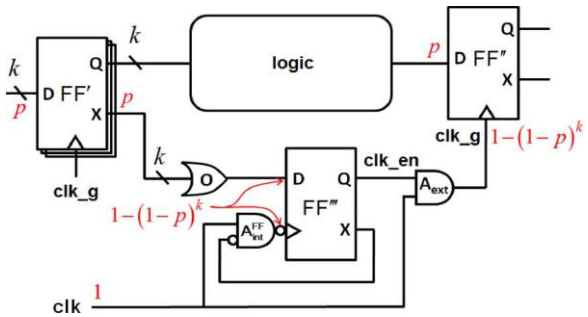
In order to over these we have a tendency to show machine Gated Flip-Flop

VI. Auto Gated Flip-Flop



The FF's master latch becomes clear on the falling fringe of the clock, where its output ought to stabilize no later than a setup time before the arrival of the clock's rising edge, once the master latch becomes opaque and conjointly the gate indicates whether or not or not the slave latch have to be compelled to change its state. If it doesn't, its clock pulse is stopped and otherwise it's passed. In [12] a big power reduction was reported for register-based tiny circuits, like counters, where the input of each FF depends on the output of its precursor at intervals the register. AGFF may also be used for general logic, but with two major drawbacks.

Firstly, only the slave latches ar gated, exploit 1/2 the clock load not gated. Secondly, serious temporal property constraints ar obligatory on those FFs residing on vital ways in which, that avoid their gating In machine gated Flip-Flop clock modify signal was generated one clock cycle ahead



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VII. Power Gating Integration

Power gating affects style design over clock gating. It will increase time delays, as power gated modes ought to be safely entered and exited. bailiwick trade-offs exist between planning for the number of run power saving in low power modes and therefore the energy dissipation to enter and exit the low power modes. motility down the blocks will be accomplished either by code or hardware.

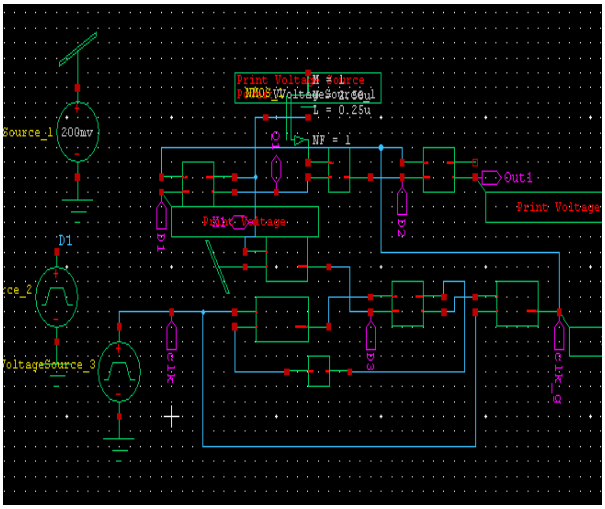

Fig: LACG with Power Gating Integration

VIII. Conclusion

In this Paper, we have a tendency to enforced the Clock gating technique integration so as to scale back the dynamic power in Flip-Flops and afterward we have a tendency to enforced the facility gating technique so as to scale back lekage power within the combinatory circuits. Power within the circuits and their performances ar evaluated with sleep technique victimization Tanner Tools.

Future scope: For Integration of clock gating we must check about the delay produced the clock gating network so in future we can design which can reduce the delay produced by the clock gating circuitry.

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