Scan-Based Delay Measurement Technique by Signature Analysis to Detect SDD: A Survey

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Abstract-This paper presents a scan-based delay measurement technique using signature registers for the small delay defect detection. The suggested method does not require the expected test vector because the test responses are analyzed by the signature registers. The overall area cost is around the conventional scan designs for design for test (DFT). The measurement time of the suggested technique is smaller than regular scan-based delay measurement. The extra signature registers can be reused for testing, diagnosis, and silicon debugging.

Keywords - Automatic Test Pattern Generation (ATPG), Design for test (DFT), Signature register(SIG), small-delay defects (SDD).

I. INTRODUCTION

When a digital system is manufactured, further testing is required to verify that it functions correctly. When multiple copies of an IC are manufactured, each copy must be tested to verify that it is free from manufacturing defects. This testing process can become very expensive and time-consuming. With today’s complex ICs, the cost of testing is an important component of the manufacturing cost. Therefore, it is very crucial to develop efficient methods of testing digital system and to design the systems so that they are easy to test. It is very crucial that a design for testability be considered early in the design process so that the final hardware can be tested efficiently and economically. Design For Testability is thus an important issue in modern IC design. Two common types of faults are short circuits and open circuits. Automatic Test Pattern Generators are employed in order to generate test sequences required for testing circuits and systems. One of the problems encountered is that normally we have access only to the inputs and outputs of the circuit being tested and not to the internal state. To remedy this issue, internal test points may be brought out to additional pins on the IC. To reduce the number of test pins required the new concept of Scan Design is introduced, in which the state of the system can be stored in a shift register and shifted out serially.

II. RELEVANCE

Various methods for the small delay defect detection have been proposed. Automatic Test-Pattern Generation (ATPG) is the process of generating patterns. Creating test patterns with a narrow path length distribution would enable testing for a small delay faults but such distributions are only found in the class of high speed random logic circuits. The majority of the designs do not fulfill this requirement. For example, the typical logic depths of video and telecom applications are 30 to 50 gates. In addition, an ATPG algorithm that targets equal path lengths would have to be paired with the actual gate and interconnect timing knowledge but this level of sophistication is well beyond the capabilities of today’s commercial ATPG tools. So other methods have to be developed to achieve this.

The path delay fault testing with a standard clock width is the most popular and widely used technique. In this method, a longer path with smaller cumulative delay due to the small delay distributed on the paths is chosen for detection. The larger the cumulative delays, the higher the probability of detection of the distributed small delay. However, the coverage of the small delay defect detection mainly depends on the normal standard clock width, which is a problem of this method. On the other hand, to solve the problem, methods of delay fault testing using a variable clock generator have been proposed. The delay fault testing with a smaller test clock reduces the slack of the paths. Therefore, the smaller delay defects that cannot be captured with the standard, clock width can be obtained with the appropriate lower test clock width.

III. LITERATURE REVIEW

A. Bulent I. Dervisoglu and Gayvin E. Stong "DESIGN FOR TESTABILITY USING SCANPATH TECHNIQUES FOR PATH-DELAY TEST AND MEASUREMENT " IEEE transactions on very large scale integration (VLSI) systems vol. 7, no . 5, Oct 1991.
Description: This paper presents techniques for using scan path techniques in testing and measuring path delays in a digital integrated circuit. Whereas scan path techniques have been used by others for detection of stuck-at type failures their use in detecting timing faults and measuring propagation delays through combinational circuit element; inside complex digital chips appear to be new the ever increasing density and functional complexity of digital integrated circuits requires more efficient and narrowly focused methodologies for testing them. Test patterns that are applied and test results that are observed directly on the input output pins of the device under test might have been sufficient to test most LSI and some VLSI components of recent vintage. This is no longer the case for present day VLSI components. There are two major components to the problem of testing modern VLSI components. First, there is the all too familiar problem of testing for stuck-at failures which manifest themselves as circuits permanently and undesirably tied to constant logic levels (logic-0 or logic-1).

Disadvantages of an existing system: An optimistic approach to achieving the above described behavior is to perform scan-in to load the internal flip-flops with a pattern other than the desired test pattern, having performed prior circuit analysis to determine that the response of the circuit to a system clock pulse shall transform that pattern into the intended test pattern. However, this is a very complicated approach to implement due to the difficulty of performing the required circuit analysis which, in effect, requires performing simulation in reverse time flow in order to determine what state the device under test should be placed in (using scan) so that its next state corresponds to the desired test pattern and the state transition between the scanned-in and final states correspond to the precise signal transitions which that are required as part of the path delay test pattern. Furthermore, since this technique allows creating signal transitions only as the combinational logic of the circuit permits, test patterns which that appear correct when internal paths are considered on their own may not be applicable when the entire circuit of the IC component is put together.

The biggest problem in doing so is the complexity of the algorithmic search necessary to determine the appropriate initial values that can be transformed by the system clock into the desired final values. Furthermore, dependencies among the circuit's inputs may make such a search very costly or prevent a successful outcome.

Advantages of an existing system: This paper describes a significant improvement to the traditional scan path methodology whereby it has become possible to measure internal path delays with high accuracy.

With this, scan path methods have been made applicable to detecting both static and timing errors in VLSI components. The techniques described here have already been used successfully to identify timing problems that were the result of a manufacturing process failure whose effects were compounded by an inadvertent physical design rule violation.


Description: With the rapid development of semiconductor technology, delay testing has become a critical problem. In Deep Sub-Micron Technology (DSM), commonly observed failure mechanisms such as resistive opens in via and interconnects, gate oxide punch through, etc. It can all lead to excessive delays on signal paths. The main types of defects that occur during the manufacturing of ICs are opens and shorts. The electrical influence of these defects strongly depends on their resistance. In general ‘Low-ohmic shorts and high ohmic' opens, cause a logic failure and are, therefore, easy to detect during testing. The detection of 'resistive shorts and opens' is harder. There is growing concern that many of these small delay defects that often escape detection at test do not accelerate sufficiently in burn-in to be detected and can cause reliability problems in the field. While traditional delay testing has primarily focused on gross delays, it is becoming apparent that "smaller" delay defects, including those on short paths, cannot be ignored. Indeed, in a 6-7 level circuit, each gate, on average, contributes about 15% of the path delay. A resistive via that increases the path delay by an additional 15% is a serious defect, even though the 15% increase in delay may be well within the timing margins employed at test, allowing the defect to pass undetected. The doubling of delay at the output of some gate because of a resistive via implies (based on a simple lumped RC model) via a resistance comparable to the driving transistor resistance, typically 1-3 Kohms. Such a large resistive defect is quite likely to degrade due to metal migration aid cause early life failure.

Disadvantages of an existing system: The difficulty in testing for the small delay defects in circuits arises from the fact that signal delays are significantly dependent on input conditions and the internal circuit channel state. Propagation delays are impacted by crosstalk, voltage drop in the power supply grid from switching activity, partial charges on internal nodes, clock skew, etc.
Sensitive delay testing requires setting up input conditions to cause worst-case delay propagation through the gate, or along the path being tested, to check if the output switches within the desired period.

Advantages of an existing system: A new delay testing method proposed here that overcomes many, if not all, of the problems in detecting small delay defects outlined. In the new Delay Detection in the Slack Interval approach, extra delays, including those on short paths, are observed by sampling outputs within the nominal clock interval. Thus, unlike the traditional delay test method, the new approach does not require the setting up of worst-case signal propagation conditions for a fault to be detected. As long as the fault is active along the signal path, it is detected. For a combinational circuit, this is done by observing the outputs at multiple time intervals, each progressively shorter than the nominal switching delay of the logic block. For practical scan based circuits, this translates to capturing the test responses to a delay test pattern at multiple fast clocks, each higher than the nominal operational clock rate. To normalize for parameter variations from the fabrication process, the test results are not evaluated against any predetermined expected response, but by comparing them with those for matched neighboring circuits from the wafer that can be expected to display similar performance.

C. Mahmut Yilmaz, Krishnendu Chakrabarty Mohammad Tehranipoor "TEST-PATTERN GRAD AND PATTERN SELECTION FOR SMALL-DELAY DEFECTS"-IEEE transactions on very large scale integration systems Vol. 19, no. 9, Nov 2008

Description: A test-grading technique is present to hold the method of output deviations for screening small delay defects (SDDs). A new gate-delay defect probability measure is defined to model delay variations for nanometer technologies. The proposed technique intelligently selects the best set of patterns for SDD detection from an n-detect pattern set generated using timing-unaware automatic test-pattern generation (ATPG). For the same pattern count, the selected patterns are more efficient than timing-aware ATPG for detecting small delay defects caused by resistive shorts, resistive opens, and process variations. Small delay variations induced by crosstalk, process variations, power supply noise, as well as resistive opens and shorts can potentially cause timing failures in a design, thereby leading to quality and reliability concerns.

However, very deep sub-micron (VDSM) technologies are especially susceptible to process variations, crosstalk noise, power-supply noise, and defects such as resistive shorts and opens, which induce small delay variations in the circuit components. Such delay variations are referred to as Small Delay Defects (SDDs) in the literature.

Disadvantages of an existing system: Test-pattern reordering methods, which rank test patterns and place the most efficient test patterns at the top of the reordered test sequence, promise reductions in both testing time and test data volume. Applying the most effective patterns first during volume ramp-up increases the likelihood of detecting manufacturing defects in less time. Test pattern reordering is also necessary for time-constrained and wafer sort environments. The reordered test set can be simply truncated to fit test-data-volume and test-time budgets.

Advantages of our an existing system: They have presented a test grading technique, based on output deviations, for screening small delay defects (SDDs). They have defined the concept of output deviations for pattern pairs and shown that it can be used as an efficient surrogate metric to model the effectiveness of Transition Delay Fault (TDF) patterns for SDDs. They have introduced a gate delay defect probability measure to model delay variations for nanometer technologies.

D. Tsung-Yeh Li, Shi-Yu Huang, Hsuan-Jung Hsu, Chao-Wen Tseng, Chih-Tsun Huang, Jenn-Chyou Bor, and Cheng-Wen Wu "AF-TEST: ADAPTIVE-FREQUENCY SCAN TEST METHODOLOGY FOR SMALL-DELAY DEFECTS"-IEEE transactions on very large scale integration (VLSI) systems, vol. 7, no. 5 Oct 2008.

Description: Small delay defects, when escaping from traditional delay testing, could cause a device to malfunction in the field. To address this issue, an adaptive frequency test method has been proposed, abbreviated as AF-test. In this way, versatile test clock scan can be generated on the chip by embedding an All-Digital Phase-Locked Loop (ADPLL) into the circuit under test (CUT). Instead of measuring the exact propagation delay associated with each test pattern like previous time-consuming failing frequency signature-based analysis, they test only up to three different test clock frequencies test for each test pattern to provide the benefit of fast characterization, and thereby making it suitable for volume production test. There are two primary strategies for delay testing.
One is the at-speed functional test. It uses functional patterns to test the chips at the target operating frequency. Even though this is an efficient method for delay testing and does not cause overkill, the growing gate count makes it harder to develop high-quality functional test. For a new microprocessor, it was reported that three man-years might be needed just to complete the functional test set. The other delay testing method is the at-speed scan test, also known as AC scan test. There are mainly two types of fault models for generating AC scan test patterns: path delay fault model and the transition fault model. Our method is primarily based on the transition fault model due to its wide adoption in the industry. For traditional transition-fault pattern generation, once a fault is propagated to an output, it will be considered as detectable.

Disadvantages of an existing system: Due to the unequal path lengths within a circuit, each path would have different timing slacks for the same test clock period. Since a delay fault cannot be detected unless it causes a path delay exceeding the test clock period a small delay defect located in a short path with a larger slack could escape the detection. Therefore, some researchers have tried to solve this problem by choosing the better paths to propagate the transition faults. The authors combine the information of Standard Delay Format (SDF) files into the ATPG tool. Then, they generated the transition fault patterns by propagating the faults through the longest paths. The authors proposed a metric called output deviation to guide the test pattern generation process in a more efficient way.

Even though these approaches could solve the problem of the small delay defects detection to some extent, they do not provide adequate resolution. In turn, there are many other researchers trying to improve the quality of delay testing from the perspective of how the test is applied. The authors proposed to use a test frequency slightly higher than the target operating frequency to increase the defect coverage. They defined the additional performance requirement as test margin.

Advantages of our proposed system: The authors used two test pattern sets for delay testing. Firstly, they test the chip at tighter frequencies with one test pattern set. If the chip fails, then they test the chip with both of the test pattern sets at target operating frequency. Otherwise, the chip is considered to have passed the test. The authors proposed to observe the variation of output delays within a group of neighboring dies. If a chip is an outlier from its adjacent dies, then it will be considered to have a delay fault. The authors proposed a method to overcome the shortage of transition fault testing by dividing test patterns into different bins.

Each test pattern is classified according to its longest path length. Patterns with similar lengths would be categorized into the same bin. After that, the authors test each bin with a particular test frequency to take into account the different slacks of different transition fault patterns.

Advantages of an existing system: They have successfully demonstrated the AF test on an in-house wireless test platform called HOY system using fabricated chips. This method can not only detect small delay defects actually but also provide a grading scheme for those marginal chips that might have the reliability problem.

IV. PROPOSED SYSTEM

The proposed method is scan-based delay measurement. The difference from the basic one is the usage of the signature registers and the additional latches for the acceleration of the delay measurement. The signature register compresses the output data into a short string of bits called a signature, and this signature is compared with the signature of a correctly functioning component. In testing a sequential circuit, as the number of inputs and states in the circuit increases, the number and length of the required test sequence increases rapidly, and the derivation of these test sequences becomes much more difficult. This in turn, means that the time and expense necessary to test the circuits increases rapidly with the number of inputs and states. The problem of testing a sequential circuit is greatly simplified if we can observe the state of all the flip-flops instead of just observing the circuit outputs. For each state of the flip-flops and for each input combination, we need to verify that the circuit outputs are correct and that the circuit goes to the correct next state. One approach would be to connect the output of each flip-flop within the IC being tested to one of the IC pins. Since the number of pins on the IC is very limited, this approach is not very practical. So the question arises: How can we observe the state of all flip-flops without using up a large number of pins on the IC? If the flip-flops were arranged to form a shift register, then we could shift out the state of flip-flops bit by bit using a single serial output pin on the IC. This leads to the concept of Scan path testing. In the proposed method, the clock width should be reduced continuously by a constant interval. Therefore, an on-chip variable clock generator is indispensable for the proposed method.

Advantages of Proposed System: In proposed system does not use the large sized multiplexers but uses scan chain and limited length extra wires. Therefore, it has less possibility of degradation of the performance of normal operation.
The embedded delay measurement approach can measure a path per a test vector. Therefore, the analysis time increases as the number of the measured path.

V. DELAY MEASUREMENT SYSTEM

Figure 1. Delay Measurement System

Figure 1 shows the block diagram for Delay Measurement System. The system consists of the low-cost tester and the chip with the Variable Clock Generator (VCG) and a BCD decoder.

The chip is assumed to have single functional clock in the proposed method, and the chip has two reset lines for initializing the flip-flop and the signature registers independently. The low-cost tester controls the whole measurement sequence. The clock frequency \( tck \) is slower than the functional clock. The line retrieves the signature data from the signature registers to estimate the measured delay.

The line \( sci \) sends the test vectors to the scan input of the chip. The line \( sco \) gets the data of the flip flop from the scan output of the chip. In the proposed measurement sequence, \( sco \) is not used. However, it is used to check the flip-flop or the additional latches before the measurement. The line \( cs \) is the clock control line.

The proposed measurement uses both the slow tester clock \( tck \) and the fast double pulse generated by on-chip VCG. The line \( cs \) selects the slow and fast clock. If \( cs \) is 1, the fast clock is sent to the \( clk \) clock line of the components. Otherwise, the slow tester clock \( tck \) is sent. The lines \( trg \) and \( cnt \) are the input lines for VCG. The fast double pulse is launched synchronizing with the positive edge of \( clk \). The line \( cnt \) controls the width of the double pulse. The line \( lck \) controls the latches for storing test vectors. The lines \( scj_0 \)……..\( scj(l-1) \) are the inputs for the encoded data to monitor the capture operation of the signature registers. The line \( se \) controls the scan flip-flops. The \( sge \) is the enable signal for the signature registers. The BCD decoder decodes the encoded input data to the control data of the signature registers \( sck_0 \)……..\( sck(m-1) \). The decoder is used to reduce the input lines for the control data of the signature registers. The flip flops in the chip are classified into the clusters \( clo \)……..\( cm(m-1) \).

VI. HARDWARE AND SOFTWARE REQUIREMENTS

A. Software Requirement

*Modelsim 6.4c*: ModelSim is a simulation tool for hardware design which provides behavioral simulation of a number of languages, i.e., Verilog, VHDL, and System C. Verilog HDL is an industry standard language used to create analog, digital, and mixed-signal circuits. HDL’s are languages that are used to describe the functionality of a piece of hardware as opposed to the execution of sequential instructions like that in a regular software application.

*Xilinx 13.2*: Xilinx Tools is a synthesize tools used for the design of digital circuits implemented using Xilinx Field Programmable Gate Array (FPGA). Digital designs can be entered in various ways using the above CAD tools: using a schematic entry tool, using a hardware description language (HDL) – Verilog or VHDL or a combination of both.

B. Hardware Requirement

*FPGA*: Field Programmable Gate Arrays (FPGAs) are programmable semiconductor devices that are based on a matrix of Configurable Logic Blocks (CLBs) connected through programmable interconnects.
As opposed to Application Specific Integrated Circuits (ASICs), where the device is custom built to the particular design, FPGAs can be programmed to the desired application or functionality requirements. Although One-Time Programmable (OTP) FPGAs are available.

Spartan 3: The Spartan 3 trainer is useful to realize and verify digital designs. User can construct Verilog/VHDL code and verify the results by implementing physically into the target device (FPGA). With the help of this kit, user can simulate / observe various input and output conditions to verify the implemented design.

VII. ADVANTAGE

The proposed method does not require the expected test vector because the test responses are analyzed by the signature registers. The measurement time of the proposed technique is smaller than conventional scan-based delay measurement.

VIII. CONCLUSION

The presented measurement technique is based on signature analysis, for screening small delay defects. Latches for short measurement time and an on-chip variable clock generator for double pulse width in scan design will be generated and compared with standard scan design. The introduced scan design achieves complete on-chip delay measurement in short measurement time using the proposed delay measurement technique and extra latches for storing the test vectors.

REFERENCES

[8] Tsung-Yeh Li, Shi-Yu Huang, Hsuun-Jung Hsu, Chao-Wen Tzeng, Chih-Tsun Huang, Jing-Jia Liou, Hsi-Pin Ma, Po-Chium Huang, Jenn-Chyoubor, and Cheng-Wen Wu “Af-Test: Adaptive-Frequency Scan Test Methodology For Small-Delay Defects” IEEE transactions on very large scale integration (VLSI) systems, vol. 7, no. 5, Oct 2008