FPGA Implementation of an Efficient Vedic Multiplier

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Abstract— Multipliers are the most significant components in the design of many high performance FIR filters, image and digital signal processors in the upcoming digital world. Multipliers being the most area and power consuming elements of a design, area-efficient low-power multiplier architectures are in demand. In this paper, multiplier based on ancient Vedic mathematics technique has been proposed which employs full adders, compressors and other efficient components to achieve the desired parameters for the proposed design.

Combining the Vedic Sutras - urdhva tiryagbhyam sutra and efficient compressors, a robust speed and area efficient multiplier architecture is achieved. The proposed multiplier is designed in VHDL and simulated using Xilinx and Modelsim softwares.

Keywords— Vedic mathematics, Xilinx, Compressor, Urdhva tiryakbhyam sutra.

I. INTRODUCTION

Vedic mathematics is the name given to the ancient system of mathematics which was used by people to calculate the problems of mathematics mentally and with high speed. Vedic mathematics is based on one of the four Vedas, ie., on the Atharvaveda. This system is based on 16 sutras by which any mathematical problem can be solved. Using one of this sutra an efficient Vedic multiplier can be designed.

II. URDHVA-TIRYAGBHYAM

Urdhva tiryagbhyam[1] is the general formula applicable to all cases of multiplication and also in the division of a large number by the other large number. Hence in VLSI applications this sutra can be used to design a vedic multiplier which has better design parameters since the number of iterations in the process of multiplication using urdhva sutra is very less and it also overcomes the drawbacks of Nikilam sutra[1] which is used to design a multiplier prior to this proposed multiplier. The sutra is explained as follows:

Multiplication of two 2 digit numbers.

For instance consider an example 14*12

Step 1: The right hand most digit of the multiplicand, the first number(14) i.e, 4 is multiplied by the right hand most digit of the multiplier, the second number(12)i.e.2. The product 4*2=8 forms the right hand most part of the answer.

Step 2: Now diagonally multiply the first digit of the multiplicand (14)i.e, 4 and second digit of the multiplier(12)i.e, 1(answer 4*1=4); then multiply the second digit of the multiplicand i.e,1 and first digit of the multiplier i.e,2(answer 1*2=2); add these two i.e, 4+2=6. It gives the next i.e, second digit of the answer. Hence, second digit of the answer is 6.

Step 3: Now, multiply the second digit of the multiplicand i.e, 1 and second digit of the multiplier i.e, 1 vertically, i.e,1*1=1. It gives the left hand most part of the answer.

Thus the answer is 168.

An alternative method of multiplication using Urdhva tiryakbhyam Sutra is shown below. The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero.

III. 3-2 COMPRESSOR

The 3-2 compressor has 3 inputs X1, X2 and X3 and 2 outputs Sum and Carry [5]. The 3-2 compressor can also be employed as a full adder cell, when the third input is considered as the Carry input X3 = C in.
The 3:2 compressor performs the same operation of a full adder but with reduction of a gate. This aims at offering high speed and less power consumption.

IV. DESIGN OF PROPOSED VEDIC MULTIPLIER

In the proposed method an Vedic multiplier using urdhva sutra is designed and further an compressor is interfaced with the urdhva multiplier to reduce the area and other parameters like number of LUTs and slices.

The proposed design uses compressors instead of full adders and hence the number of gates used is also reduced. The design of the proposed Vedic multipliers is as follows.
V. IMPLEMENTATION OF VEDIC MULTIPLIER

The proposed multiplications were designed in VHDL and implemented using XILINX and MODELSIM softwares and Vedic technique is compared with existing conventional array multiplier, Wallace tree multiplier and multipliers using compressor. It is evident that there is a considerable increase in speed and area of the Vedic architecture. The simulation results for Vedic multipliers are shown in the figures below.

![First level RTL schematic diagram of 8*8 Vedic multiplier](image)

a) 8*8 Vedic multiplier (urdhva) using array multiplier

![Second level RTL schematic diagram of 8*8 Vedic multiplier](image)

b) 8*8 Vedic multiplier(urdhva) using compressor

c) First level RTL schematic diagram of 8*8 Vedic multiplier

d) Second level RTL schematic diagram of 8*8 Vedic multiplier
e) Third level RTL schematic diagram of 8*8 Vedic multiplier.

f) FPGA implementation.

Table-1 shows the synthesis result for various design implementations. The result obtained from proposed Vedic multiplier is better than any other existing multiplier and the delay is noted to be 48.32 ns for the Vedic multiplier using array multiplier and also the number of LUTs is very less, it is reduced by 45 LUTs (reduced from 736 to 691) in the case of proposed Vedic multiplier using compressor.

VI. CONCLUSION

The designs of 8*8 bits Vedic multiplier have been simulated using XILINX AND MODELSIM SOFTWARE and implemented using SPARTAN3. The design is based on Vedic method of multiplication. It is therefore seen that the Vedic multipliers are much more faster than the conventional multipliers. This gives us method for hierarchical multiplier design. So the design complexity gets reduced for inputs of large no of bits and modularity gets increased. Urdhva tiryakbhyam, Nikhilam and Anurupye sutras are such algorithms which can reduce the delay, power and hardware requirements for multiplication of numbers. Thus for an application which requires a less delay multiplier Vedic multiplier using array multiplier as a component can be chosen and for applications requiring less number of LUTs, area and less number of gates the Vedic multiplier using compressor can be used.
FPGA implementation of this multiplier shows that hardware realization of the Vedic mathematics algorithms which is verified using SPARTAN3. The high speed multiplier algorithm exhibits improved efficiency in terms of speed.

REFERENCES


