International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 7, Issue 3, March 2017)

Design & Implementation of Digital to Digital Converter Comprising Ternary Logic to Binary Logic

Vinay U. Kale [1], Vijay T. Ingole [2], Ashwin K. Thakur [3]
[1]*Professor, Dept. of EXTC, PRMIT & R, Badnera, Amravati, India*
[2]*Director, DRGIT & R, Amravati, India*
[3]*Asst. Professor, Department of EXTC, DRGIT & R, Amravati, India*

***Abstract*— The structural design & realization of Ternary to Binary converter is described. The objective of this converter is to suggest a solution for compatibility between Ternary & Binary systems. The suggested Ternary to Binary converter is implemented using 4 trit of Ternary logic into fraction of 5 bit Binary logic conversion. Aforesaid Ternary to Binary converter provides a fast method for digital conversion from Ternary to Binary logic. Ternary signals are used as an input for the converter which converts Ternary signals into Binary signals using matrix of MOSFET devices. Binary logic gates are implemented for switching the MOSFET matrix. The design is implemented using cadence schematic editor and simulated using cadence virtuoso analog design environment at 180nm CMOS process technology.**

***Keywords*— Binary, CMOS, Converter, MVL, Ternary.**

I. INTRODUCTION

Ternary logic is one of the emerging fields in digital electronics and computing machines. Most of the current systems work on Binary logic. Ternary logic has 3 levels which provide many advantages over existing Binary system including reduced interconnection required for implementation of logic. When an application needs higher speed of operation, Ternary logic is proved to be an excellent option [1,2,3]. Unbalance Ternary Logic system has levels 0, 1, 2 representing low, intermediate & high voltage levels [4]. The system having higher radix than 2 shows faster speed of processing in arithmetic operation as less number of digits is required [5,6]. The channel capacity can be utilized more effectively as higher information content can be processed [7,8].

For the compatibility of Binary logic system & Ternary logic system [9], a Ternary Logic to Binary Logic converter is essential.

For 'n' trit Ternary system, total 3n digital combinations are possible and for 'm' bit Binary system, total 2m digital combinations are possible.

Hence,

$$n*\log 3 = m*\log 2$$

$$\frac{m}{n} = 1.58$$

For example an n=32 trit Ternary system and a 32 bit Binary will have counting ratio 332/232 = 431440. This means 32 digit Ternary based systems will process the information 431440 times more than contemporary 32 bit Binary computer architecture [10, 11].

II. TERNARY DECODER

The Ternary decoder is composed of three different Ternary switches where padding of two MOS transistor [12] is implemented as shown in Fig.1. This decoder is composed of total 10 transistors. Threshold voltage of switches is adjusted by padding of MOS transistors. By padding of PMOS in switch1, the input falls to low level. On the other hand if NMOS is considered the input is raised to high level. The desired Ternary logic level is obtained by changing the threshold voltage of the transistor.

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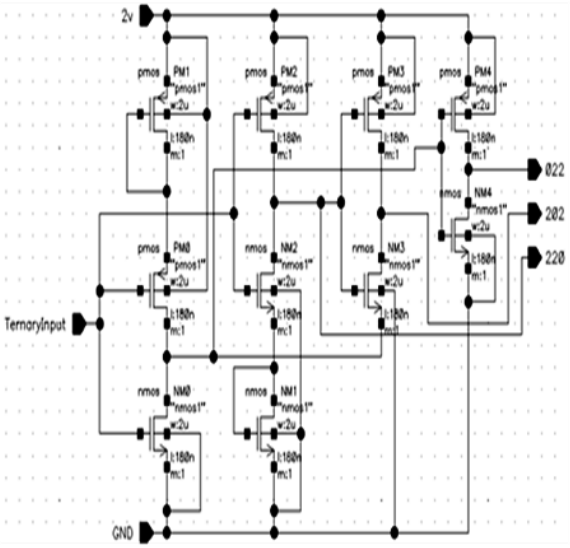

Fig.1: Ternary Decoder

III. Ternary To Binary Converter

Ternary to Binary converter is shown in Fig.2. Ternary decoder gives two level output. This output of Ternary decoder is used to switch the MOSFET matrix to obtained desired output. For this purpose the standard decoder circuit is used. The decoder circuit consists of NOR gate & an inverter. As the Ternary input is applied to the decoder, corresponding gate will become ON & corresponding MOSFET matrix converts it into Binary output. As shown in Fig.2 the decoder circuit uses Ternary input. Output of decoder has two levels 0 & 2. These outputs are applied to the Ternary to Binary converter which drives the matrix of MOSFET producing desired output.

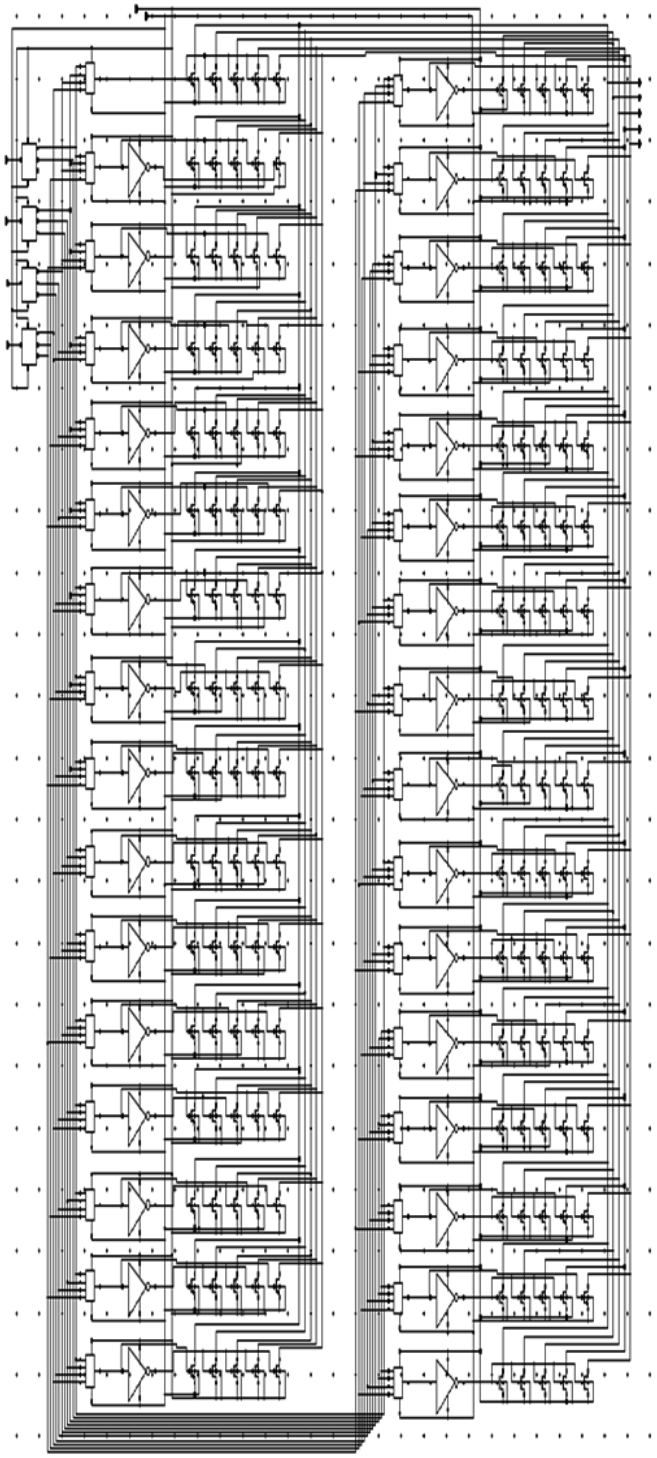

Fig.2: 4-trit Ternary to 5-bit Binary Converter

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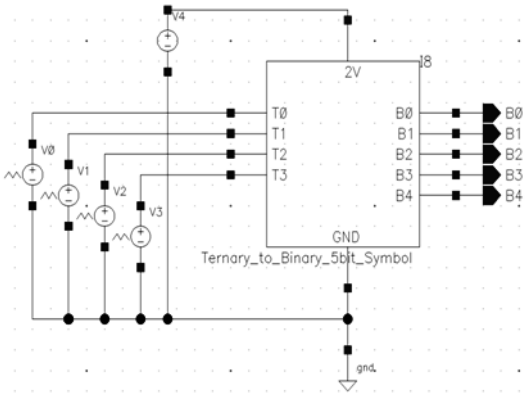

Fig.3: Block Diagram of Ternary to Binary Converter

IV. Simulation Results

The implementation of proposed Ternary to Binary converter is illustrated in Fig.3. Cadence schematic editor and Cadence virtuoso analog design environment is used for simulation. The desired outputs of above designs are shown in Fig.4. Though the circuit implementation shows unbalanced Ternary logic levels 0, 1 & 2 Volt, it is equally applicable to balance Ternary logic circuit represented by -1, 0, +1 levels. The output obtained is in the form of Binary 0 & 2 Volt corresponding to logic 0 and 1 level.

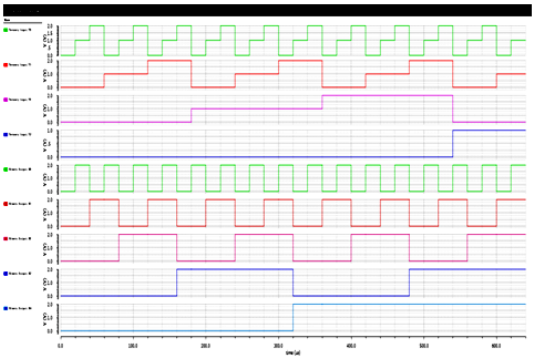

Fig.4: 4-trit Ternary to 5-bit Converter Input & Output Waveforms

V. Conclusion

The proposed Ternary to Binary converter is designed & simulated successfully. Ternary input is applied to the converter & desired Binary output is obtained. The proposed design is simple and offers a fast conversion of Ternary logic system into Binary logic system.

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