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Ultra Low Power Dissipation in Adiabatic Logic Circuits in DSM Technology

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***Abstract*— CMOS technology is scaling down to meet the performance, production cost, and power requirements of the microelectronics industry. The increase in the transistor leakage current is one of the most important negative side effects of technology scaling. Leakage affects not only the standby and active power consumption, but also the circuit reliability, since it is strongly correlated to the process variations. Leakage current influences circuit performance differently depending on: operating conditions (e.g. standby, active, burn in test), circuit family (e.g. logic or memory), and environmental conditions (e.g. temperature, supply voltage). However, this progress help in rapid run towards tiny, circuit design high speed and economical VLSI (Very Large Scale of Integration) circuits has added to excessive power dissipation of numerous circuits used today. The main contribution of this paper is to analyse and compare different adiabatic logics like PFAL logic circuits and design a novel proposed logic circuit, to mitigate power consumption, Delay, PDP with the variation of Frequency range from 10MHz to 1GHz. All simulations are performed by using BSIM4 model HSPICE by using 65nm technology. Finally average power dissipation characteristics are plotted with the help of graphs and comparisons are made between PFAL logic family and new proposed PFAL logic family.**

***Keywords:-* C-CMOS, ECRL, 2N-2N2P, Power, Delay, Low power.**

I. INTRODUCTION

The tremendous increase in the transistor leakage current is the primary disadvantage of technology scaling. Leakage affects not only the standby and active power consumption, but also the design margins, since it is closely related to process variations [1-2]. As a result, it is vital for a circuit designer to be aware of the impact of leakage on the operation of the circuit and techniques to mitigate it. Leakage current affects the circuit differently depending on the operating conditions (e.g. standby, active and burn in test), circuit family (e.g. logic or memory) and environmental conditions (e.g. temperature and supply voltage). Consequently, specific solutions exist for the particular condition of the circuit that it is being applied to. Principally, the focus of this work is on techniques that mitigate leakage in circuits operating in the active mode with various temperatures and supply voltages.

Since there is no single technique that will deal with all sources of leakage and their impact simultaneously, this problem must be tackled at various levels [3]. So there exist solutions that will address leakage current at the system, circuit and device level. The circuit level solution is chosen for investigation in this work. The three main components of MOS transistor leakage are gate, subthreshold and junction tunneling leakage. Presently, subthreshold leakage is the dominant component of the total leakage in current manufacturing technology nodes and it will remain to be the dominant component even at the lower technology nodes at higher than room temperatures [4]. There are several different techniques that tackle these leakage components in various angles. Some of these techniques only focus on component, whereas others address more than one component at the same time. Also, some techniques might reduce one component of the MOS leakage but they might increase the other components. Therefore it is advantageous to know the limitations of each of these techniques, and their effectiveness in the lower technology nodes.

Adiabatic Switching

The principle behind adiabatic switching is that, the transitions should be sufficiently slow so that heat is not emitted significantly. This slow transition is achieved when DC power supply is replaced with an AC power clock which can be achieved by a resonance LC driver, an oscillator, a clock generator etc[8] . As we know that, a constant charging current source corresponds to a linear voltage ramp. If the constant current source delivers the charge Q (= CV_{dd}) during the time period T, the energy dissipated in the channel resistance R is given by-

$$E_{diss} = I^2RT = \left(\frac{CV_{dd}}{T}\right)^2 RT = \left(\frac{RC}{T}\right)CV_{dd}^2 \qquad (3)$$

From the equation, as the T is increased linearly, power dissipation will decrease linearly. If T is made sufficiently larger than RC, the energy dissipation will be nearly zero. This is the principle of adiabatic switching.

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II. ADIABATIC LOGIC

Conventional static CMOS circuits suffer the inevitable energy loss (CV^2_{DD}) at each charging and dis- charging operations. In the charging operation, the energy dissipation from power supply through pull-up PMOS block is CV^2_{DD}. $0.5CV^2_{DD}$ energy is stored in load capacitance. The other half of the energy is dissipated in the resistive path, and converted to heat. During the discharging operation, the residual $0.5CV^2_{DD}$ energy stored in the capacitance is released through pull-down NMOS block to the ground terminal. Therefore, no energy can be recovered in the conventional CMOS circuit. Adiabatic circuits employ AC power source (clock) rather than the DC supply, and therefore can recover the energy stored in capacitance back to the power source, and completely avoid the dynamic power dissipation theoretically. In adiabatic logic, the node voltage changes synchronously [5-8].

Usually the adiabatic circuit operation consists of four phases, namely Wait, Evaluate, Hold and Recover. The phase difference between adjacent phases is a quarter of period. Here in Figure 1, the simplest adiabatic buffer with 2N2P structure, which contains two cross-coupled P-MOSFETs and two differential input N-MOSFETs, is taken as an example to explain the four-phase operation mode [2]. The N-MOSFETs block is the evaluation logic and the P-MOSFETs are the charging and discharging current access of the adiabatic logic. The typical time sequence of the 2N2P logic is also shown in Fig. 1. The four-phase operations are shown as follows:

1) Wait: The power supply stays zero, the inputs become valid and the evaluation logic generates pre-evaluated result and the outputs keep low voltage.

2) Evaluate: The power supply rises from zero to VDD gradually, and inputs remain stable. According to the result of pre-evaluation, output follows the power supply to become valid.

3) Hold: The power supply stays high to keep the output valid, providing the constant input signal for the next stage in the adiabatic pipeline. Besides the inputs return to zero.

4) Recover: The power supply climbs down to zero. The remaining zero voltage inputs shut down the current access to the ground; thus the charge stored in the node capacitance can flow back to the power supply through the cross-coupled P-MOSFETs.

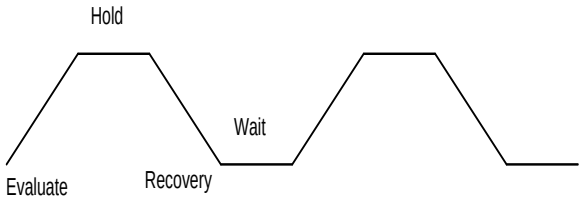

Fig. 1: Four Phased Trapezoidal Power Clock

The most widely used adiabatic logics include 2N2N2P, IPAL, PFAL and DCPAL. Above four types adiabatic buffers as shown in Fig.2. They have similar operations with 2N2P logic but also have some differences. In the 2N2N2P logic, the two more N-MOSFETs with P-MOSFETs make up two inverters to cross-couple, which increases the stability of the outputs. The IPAL logic folds the evaluation logic upward to the pull-up blocks to form two charging paths with a pair of cross-coupled P-MOSFTEs, which reduces the time taken to evaluate the outputs [9-10]. Based on the IPAL logic as shown in Fig.4, The PFAL logic adds a pair of feedback N-MOSFETs, and the feedback signal comes from the next stage's outputs. This structure effectively eliminates the charge stored in the output node after the recovery phase, which can provide complete charge recovery. DCPAL adds a gating N-MOSFET in the pull-down path to reinforce the suppression of leakage current. To sum up, considerable dynamic power reduction can be realized by adiabatic circuit. However, with the aggressive scaling of devices technology, the leakage power becomes more and more serious. Hence, leakage current should be carefully considered in the adiabatic circuit design [11-13].

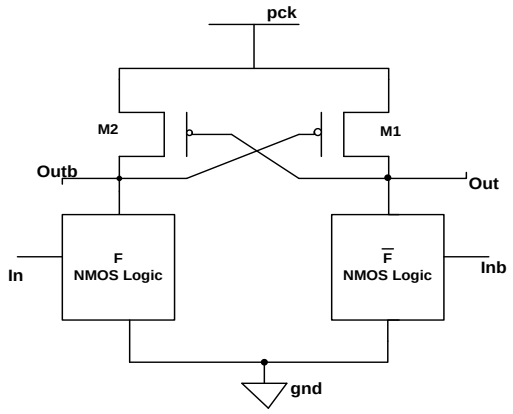

Fig. 2: Efficient Charge Recovery Logic (ECRL)

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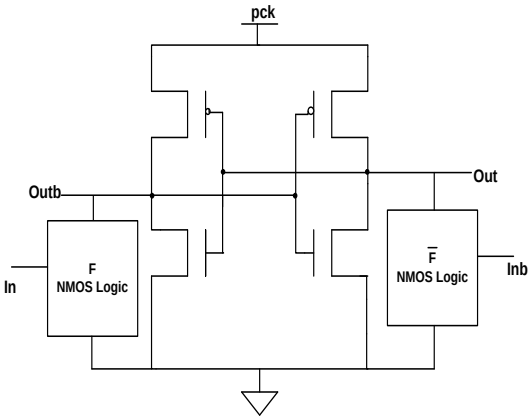

Fig. 3: 2N-2N2P Basic Logic circuit

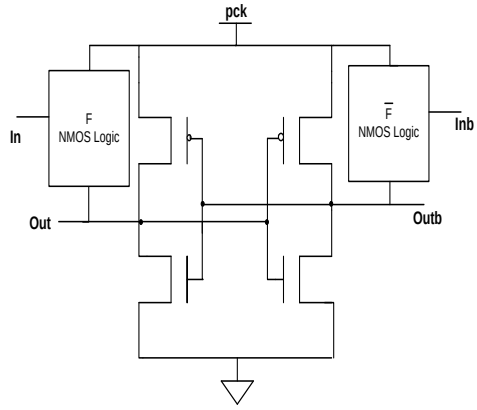

Fig. 4: PFAL Basic logic circuit

III. PROPOSED CIRCUIT

For the operation of adiabatic logic, the charging and discharging processes merely depend on the pull-up transistors, while the pull-down transistors primarily serve to accelerate the cross-coupling and maintain the certain nodes at zero voltage. Therefore the working speed of adiabatic circuits is determined by the pull-up transistors, independently of the pull-down parts. However the pull-down transistors have great influences on the leakage current; it decides the power consumption.

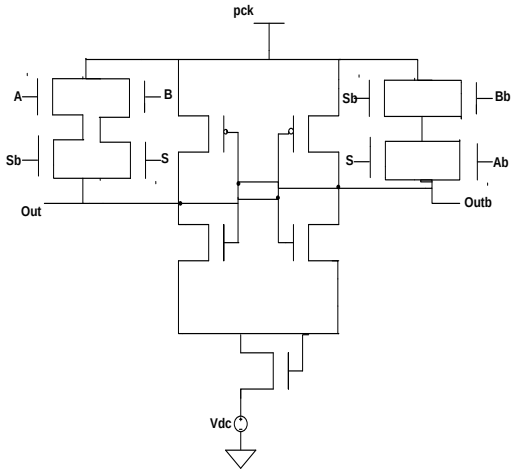

Fig.5: Propsed PFAL Adiabatic Logic

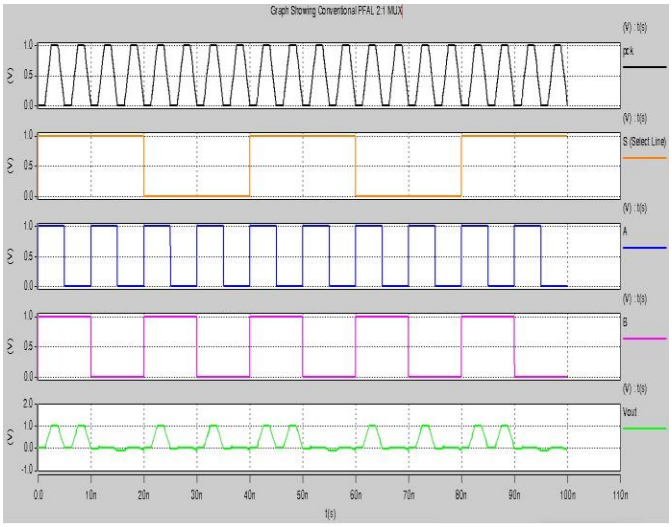

Fig. 6: Input/ Output waveforms for PFAL 2:1 MUX at 100MHz.

The functional blocks of NMOS logic are connected in parallel with the PMOS transistors of the latch forming the transmission gates similar to PFAL logic. The difference lies in the pull-down block with an NMOS diode and a DC voltage source connected between the pull-down NMOS transistors and the ground.

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The idea behind use of a diode at the bottom of NMOS tree is that it will help in controlling the discharging path by decreasing the rate of discharge of internal nodes of the logic circuit. And to further incorporate the advantage of level shifting technique, a positive DC voltage source is connected between the diode and the ground.

IV. Results And Disscusion

For further verification and demonstration, in this section the power dissipation of various basic adiabatic logic standard cells based on ICPAL has been investigated. The evaluation logic of 2N2N2P and IPAL is standard CMOS logic while CPAL and ICPAL employ CPL as evaluation logic. PTM is used for 32 nm FinFET devices and all of the simulations are based on HSPICE. The size (W/L ratio) of the transistors (N-MOS and P-MOS, respectively) is set to be the same, so that the comparison of power dissipation between different types of adiabatic circuits is distinct. Since the clock signal is periodic and each period has four phases, the given inputs are also periodic and their periods are integral multiples of the clock period. The average power dissipation in each period of inputs is measured as the characteristic power dissipation of the certain adiabatic logic cell. Here, the influence of different inputs on power dissipation is also considered and we average the power dissipation under the condition of different inputs as the final experimental results. As the Power consumption at different Frequency is Shown in Fig.7, 8 and 9 as the frequency increases the power consumption of the circuit also increase.

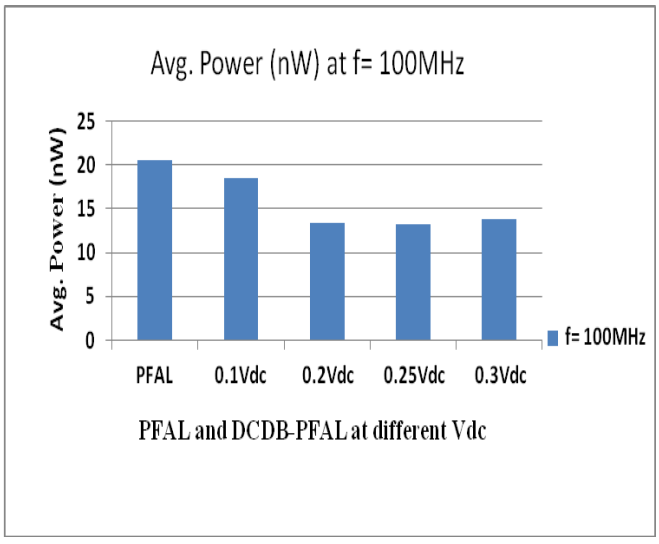

Fig. 7: Avg. Power comparison of conventional PFAL vs. proposed DCDB-PFAL at 100MHz.

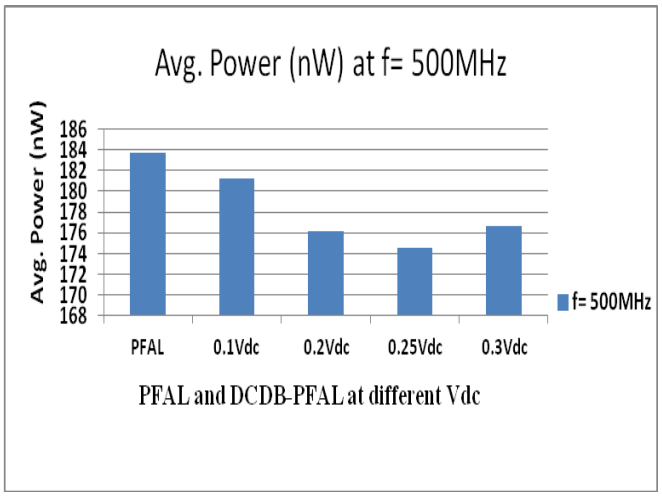

Fig. 8: Avg. Power comparison of conventional PFAL vs. proposed DCDB-PFAL at 500MHz.

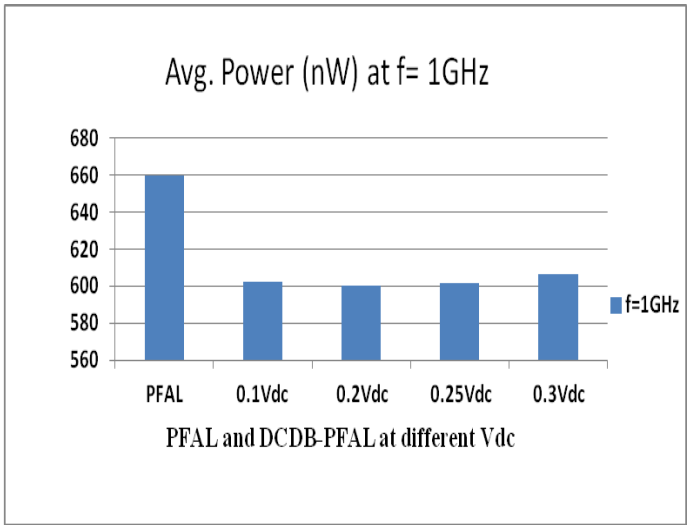

Fig. 9: Avg. Power comparison of conventional PFAL vs. proposed DCDB-PFAL at 1GHz.

V. Conclusion

A novel ICPAL has been proposed for ultra-low power dissipation applications. For demonstration and verification, various adiabatic logiccells based on ICPAL have been investigated compared with other conventional adiabatic logics.

The experimental results indicate that the power dissipation of ICPAL circuits is much lower than that of other conventional adiabatic circuits (the reduction is about 23.1% for 2N2N2P, 75.0% for IPAL, and 50% for CPAL, respectively) in the similar number of transistors. ICPAL circuits also support a better pre-evaluation of system power dissipation in VLSI design and have an intrinsic characteristic for the resistance to some types of SCAs.

REFERENCES

[1] Philip Wong, H.S., D. J. Frank., P. M. Solomon, C. H. J. Wann And J. J. Welser. Nanoscale Cmos. In: Proc. Of Ieee, 1997 , Vol. 87, Iss. 4, pp. 537–570.

[2] Nowak, E. J., I. Aller, T. Ludwig, K. Kim, R. V. Joshi, C-T. Chuang And R. Puri. Turning Silicon On Its Edge. IEEE Circuits & Device Magazine, 2004, Pp.20–31.

[3] Tawfika, S. A. And V. Kursun. Finfet Domino Logic With Independent Gate Keepers. Micro Electronics Journal. 2009, Vol, 40, pp. 1531-1540

[4] M.L. Keote, P.T. Karule, Design And Implementation Of Energy Efficient Adiabatic Ecrl And Basic Gates. International Conference On Soft Computing Techniques And Implementations- (Icscti), Oct 8-10, 2015.

[5] J. S. Denker. A Review Of Adiabatic Computing. In: Ieee Symposium On Low Power Electronics, San Diego, 1994. 94–97

[6] B. H. Calhoun, S. Khanna, R. Mann, Et Al. Sub-Threshold Circuit Design With Shrinking Cmos Devices. In: Ieee International Symposium On Circuits And Systems, Taipei, 2009. Pp. 2541–2544

[7] S. Hemantha, A. Dhawan, K. Haranath. Multi-Threshold Cmos Design For Low Power Digital Circuits. In: 2008 Ieee Region 10 Conference On Tencon, Hyderabad, 2008. 1-5

[8] Y. Moon And D.K. Jeong, An Efficient Charge Recovery Logic Circuit. Ieee Journal Of Solid-State Circuits, Vol. 31, 1996, pp. 514-522 As Accessed On October, 2014.

[9] A. Kramer, J.S. Denker Et Al., 2nd Order Adiabatic Computing With 2n-2n And 2n-2n2p Logic Circuits. Proc. Intern. Symp. Low Power Design, 1995, Pp. 191-196 As Accessed On September, 2014.

[10] A. Vetuli, S. Di Pascoli And L. M. Reyneri, Positive Feedback In Adiabatic Logic. Electronics Letters, Vol. 32, No. 20, Sep. 1996, Pp. 1867 As Accessed On July,2014.

[11] A. Blotti , S. D. Pascoli And R. Saletti, Simple Model For Positive Feedback Adiabatic Logic Power Consumption Estimation. Electronics Letters. Vol. 36, No. 2, Jan, 2000, Pp. 116-118 As Accessed On March, 2014.

[12] K. Roy And Y. Ye, Ultra Low Energy Computing Using Adiabatic Switching Principle. Ece Technical Reports, Purdue University, Indiana, As Accessed On April, 2013.

[13] A. Chaudhary, M. Saha, M. Bhowmik Et. Al.,Implementation Of Circuit In Different Adiabatic Logic. Ieee Sponsored 2nd International Conference On Electronics And Communication System,Icecs, 2015.