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Real Time Implementation of PV Fed IEEE Bus System Interfaced by 3-Phase 4-Leg Inverter Using OPAL-RT

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Abstract- **In recent years, with the advancement of power electronic technology, the expenses of renewable energy technology has decreased so that applications can be economically justified by utility. Renewable energy electric generations are being used increasingly interconnected in distributed network with the use of power electronic converters in reasonable way since it is placed near the load with more efficient operation. This paper represents 3-phase 4-leg interfacing inverter to interface renewable energy sources (RESs) to electric power system (EPS) in which PV is interconnected to IEEE 14 bus system. The PV system which is integrated to distributed network with 3-phase 4-leg interfacing inverter, is analyzed for voltage profile of each bus along with active and reactive power flow at each bus of IEEE 14 bus system using MATLAB/SIMULINK™ software. The real-time voltage profile, active and reactive power flow is also analyzed by OPAL-RT which is PC/FPGA based Real-Time Digital Simulator (RTDS).**

Keywords: **Renewable Energy Sources (RES), Photovoltaic (PV), Electric Power System (EPS), Point of Common Coupling (PCC), Custom Power Device (CPD), Real-Time Digital Simulator (RTDS)**

I. INTRODUCTION

Dearth of conventional fossils fuel and their higher emissions are the twin concern for centralized power generation. To meet the energy demand and to have sustainable growth and social progress, it is obligatory to utilize RESs like Solar, Wind, Hydro, Biomass, Cogeneration etc. [1].

Energy requirement cannot be meet by RESs alone since RESs can be used as hanging energy sources which will work in coordination with existing conventional plants so it is necessary to integrate power sources from renewable sources like solar and wind into power network to reduce environmental impact of already existing conventional plant such as thermal, hydral etc.

The integration of RESs adds on some power quality issues to power network such as voltage regulation, harmonic distortion, flicker, stability, distortion, etc., these power quality issues are to be confined to IEC and IEEE standards.

Due to the intermittent and unpredictable nature of sources, mainly sun or wind, integration of RESs in smart grid is a challenging task. Research in this field divulge that there may occur power quality issues at the generation, transmission and distribution [2]. IEEE-519 standard is widely accepted for power quality at the point of common coupling (PCC) with the utility grid [3]. Some remedies to these power quality problems are investigated in the literature [4]. Custom Power Devices (CPDs) are used for compensation of the power quality problems in the current, voltage and both current and voltage respectively.

Different Power Quality issue has been discussed in [5]. Researchers presented control strategy to improve PQ of electric power system (EPS) for achieving maximum benefits from grid-interfacing.

The CPDs connected to non-linear loads introduce harmonics to the grid. Therefore, to get stabilized output at PCC, the controller need to be designed for the CPDs [6],[7]. The concept of a custom power using CPDs, to provide quality power at various level. It has been extended further in [8] by using supervisory control techniques to coordinate the CPDs by proving the pre-specified quality of power. Researchers in [10],[11],[12] suggests the use of 4-leg grid interfacing inverter control to perform as a multi-function device by assimilating active filter functionally. The inverter can thus be utilized as power converter to inject power generated from RES to the grid, and shunt APF to compensate current unbalance, load current harmonics, load reactive power demand and load neutral current. This control leads to the linear/non-linear unbalanced load as balanced linear load to the grid at PCC.

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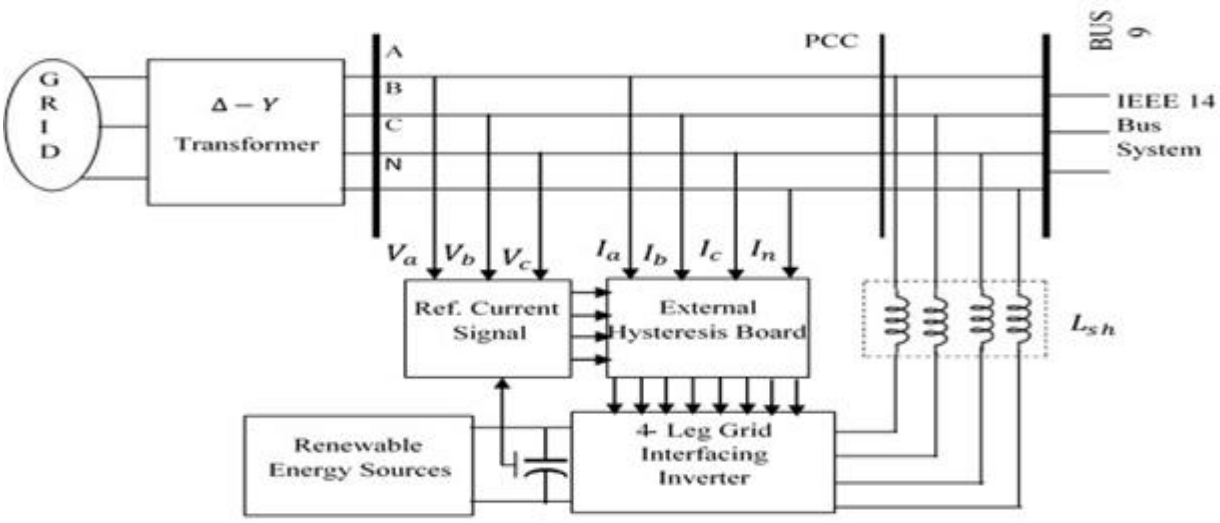

Fig.1 Schematic of Renewable Based Distributed Generation System [8],[12]

Since 4 leg VSI has advantageous over both 2 leg inverter and UPQC [9], [13], [14], [15] in terms of operating voltage and inherent property of 4th leg in compensating neutral current, hence the proposed model use 3-phase 4-leg interfacing inverter for interconnection of RES with existing grid. Hysteresis control method is being used which compare actual current and reference current of inverter to give gate pulse.

Fig.1 shows the schematic diagram of proposed RES based generation system. The proposed model is simulated by considering PV as RES for distributed generation.

OPAL-RT is PC/FPGA based Real-Time Digital Simulators, Hardware-In-the-Loop (HIL) testing equipment and Rapid Control Prototyping (RCP) systems. Real-time hardware based simulation platforms enable model execution at the same rate as actual time [16].

OPAL-RT provides a complete range of real-time digital simulators and control prototyping systems for power grids, power electronics, motor drives and other mechatronic systems. In addition, the RT-LAB, core OLAP-RT software, enables user to develop models for real-time simulation [17]. These real-time systems help to perform feasibility studies, develop new concepts, design and test controllers for a wide variety of applications including small power converters, hybrid electric drives, large power grids and renewable energy systems. Hence, OPAL-RT is a solid alternative to overpriced **R**eal-**T**ime **D**igital **S**imulators.

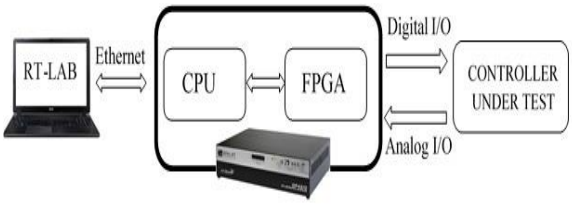

Fig.2 Schematic of OPAL-RT Implementation

In this paper, PV is integrated at bus 9 of IEEE 14 bus system and its real-time implementation is analyzed using OPAL-RT for voltage profile, active and reactive power flow.

II. Operating Principal

The single phase equivalent circuit for R phase of system is shown in Fig. 3.

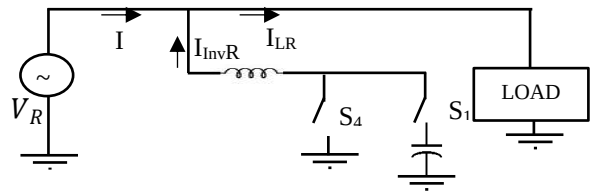

Fig.3 Single Phase Equivalent Circuit of the System and VSI

Load current for R phase can be written as

$$I_{LR} = I_{LRf} + I_{LRh} \quad (1)$$

$$I_{La} = I_{InvR} + I_s \quad (2)$$

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Where, I_{LRf} is the fundamental component and I_{LRh} harmonic component of load current. Since supply side should be free the harmonic component of load current, the inverter has to inject a current whose magnitude should be equal to harmonic component.

This condition should be satisfied,

$$I_{LRh} = I_{InvR} \quad (3)$$

From equation (2) and (3),

$$I_s = I_{LRf} \quad (4)$$

If $I_{LRh} > I_{InvR}$ S_4 should be OFF and S_1 should be ON so the current generated by dc capacitor I_{InvR} is equal to I_{LRh}. If $I_{LRh} < I_{InvR}$ S_4 should be ON and S_1 should be OFF so the current I_{Inva} should be transferred to the ground in order to have $I_{InvR} = I_{LRh}$.

III. Control Stratgy

A Phase Locked Loop (PLL) is used to extract the pure sinusoidal signal at fundamental frequency. The output of the PLL gives U_R (unit vector for phase R) which is expressed mathematically as,

$$U_R = \sin(\omega t) \quad (5)$$

The unit vector for phase Y and phase B can be obtained by proper phase shifting and is expressed as,

$$U_Y = \sin(\omega t - 120) \quad (6)$$

$$U_B = \sin(\omega t + 120) \quad (7)$$

The dc-link voltage (V_{dc}) is passed through a first-order low pass filter (LPF) in order to eliminate the switching ripples on the dc-link voltage and in the generated reference current signals. The difference of this filtered dc-link voltage (V^*_{dc}) and reference dc-link voltage is passed through a discrete-PI regulator to maintain a constant dc-link voltage under varying generation and load conditions. The dc-link voltage error $V_{\mathrm{dcerr(n)}}$ at n^{th} sampling instant is given as,

$$V_{\mathrm{dcerr(n)}} = V^*_{dc(n)} - V_{dc(n)} \quad (8)$$

The output of discrete-PI regulator at n^{th} sampling instant is expressed as,

$$I_{m(n)} = I_{m(n-1)} + K_{PVdc}\left(V_{dcerr(n)} - V_{dcerr(n-1)}\right) + K_{IVdc}V_{dcerr(n)} \quad (9)$$

Where, K_{PVdc} and K_{IVdc} are proportional and integral gains of dc-voltage regulator.

The peak amplitude (I_m) is then multiplied with unit vector templates giving reference current signals for shunt APF.

The reference three phase grid currents are enumerated as their instantaneous values as

$$I^*_R = I_m - U_R \quad (10)$$

$$I^*_Y = I_m - U_Y \quad (11)$$

$$I^*_B = I_m - U_B \quad (12)$$

The forth leg of grid-interfacing inverter compensates neutral currents if presents due to loads connected to neutral conductor since it should not be drawn from the grid. In other words, the reference current for the grid neutral current is considered as zero and can be expressed as,

$$I^*_n = 0 \quad (13)$$

The reference grid currents (I^*_R, I^*_Y, I^*_B and I^*_n) are compared with actual grid currents (I_R, I_Y, I_B and I_n) to compute the current errors as,

$$I_{Rerr} = I^*_R - I_R \quad (14)$$

$$I_{Yerr} = I^*_Y - I_Y \quad (15)$$

$$I_{Berr} = I^*_B - I_B \quad (16)$$

$$I_{nerr} = I^*_n - I_n \quad (17)$$

These current errors are given to hysteresis current controller which then generates the switching pulses (P_1 *to* P_8) for the gate drives of grid-interfacing inverter as shown in Fig. 4.

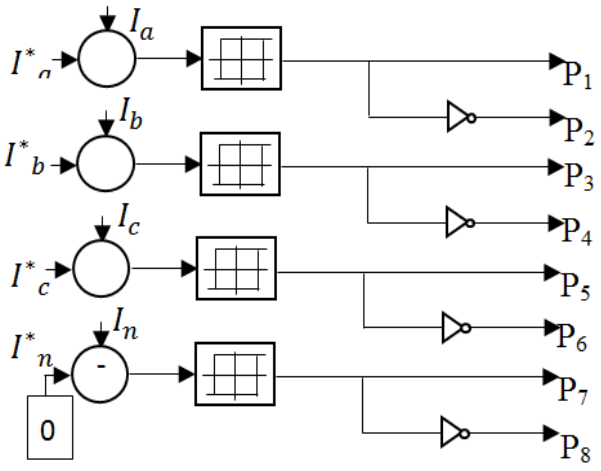

Fig.4 Gate Pulse Generation

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The average model of 4-leg inverter can be obtained by the following state space equations

$$\frac{dI_{InvR}}{dt} = \frac{(V_{InvR} - V_R)}{L_{sh}} \quad (18)$$

$$\frac{dI_{InvY}}{dt} = \frac{(V_{InvY} - V_Y)}{L_{sh}} \quad (19)$$

$$\frac{dI_{InvB}}{dt} = \frac{(V_{InvB} - V_B)}{L_{sh}} \quad (20)$$

$$\frac{dI_{Invn}}{dt} = \frac{(V_{Invn} - V_n)}{L_{sh}} \quad (21)$$

$$\frac{dV_{dc}}{dt} = \frac{(I_{InRd} + I_{InYd} + I_{InBd} + I_{Innd})}{C_{dc}} \quad (22)$$

Where, V_{InvR}, V_{InvY}, V_{InvB}, V_{Invn}, are the three-phase ac switching voltages generated on the output terminal of inverter. These inverter output voltages can be modelled in terms of instantaneous dc bus voltage and switching pulses of the inverter as,

$$V_{InvR} = \frac{(P_1 - P_4)}{2} V_{dc} \quad (23)$$

$$V_{InvY} = \frac{(P_3 - P_6)}{2} V_{dc} \quad (24)$$

$$V_{InvB} = \frac{(P_5 - P_2)}{2} V_{dc} \quad (25)$$

$$V_{Invn} = \frac{(P_7 - P_8)}{2} V_{dc} \quad (26)$$

Similarly the charging currents I_{Invad}, I_{Invbd}, I_{Invcd} and I_{Invnd} on dc bus due to the each leg of inverter can be expressed as,

$$I_{InvRd} = I_{InvR}(P_1 - P_4) \quad (27)$$

$$I_{InvYd} = I_{InvY}(P_3 - P_6) \quad (28)$$

$$I_{InvBd} = I_{InvB}(P_5 - P_2) \quad (29)$$

$$I_{Invnd} = I_{Invn}(P_7 - P_8) \quad (30)$$

The switching pattern of each IGBT inside inverter can be formulated on the basis of error between actual and reference current of inverter, which can be explained as,

a. If, $I_{InvR} < (I^*_{InvR} - h_b)$ then upper switch S_1 will be OFF ($P_1 = 0$) and lower switch S_4 will be ON ($P_4 = 1$) in the phase "a" leg of inverter.
b. If,$I_{InvR} > (I^*_{InvR} - h_b)$ then upper switch S_1 will be ON ($P_1 = 1$) and lower switch S_4 will be OFF ($P_4 = 0$) in the phase "a" leg of inverter.

Where, h_b is the width of hysteresis band. On the same principle, the switching pulses for the other remaining three legs can be derived.

IV. Mathematical Model

The proposed model consists of PV system with their MPPT so that maximum power can be tracked under given temperature and solar insolation. PV is a dc source of energy hence dc-ac converter is needed. 3-phase 4-leg interfacing inverter is designed in SIMULINK for the dc-ac conversion as well as controlling the aspects of existing grid at the instant of interconnection. The controlling action is achieved by switching pulse of IGBTs of interfacing inverter. In this paper a MATLAB/SIMULINK model is modelled in which RES is integrated to bus 9 of the existing IEEE 14 bus network. Fig.5 is the MATLAB model of interfacing inverter and Fig.6 is the model for switching pattern of interfacing inverter.

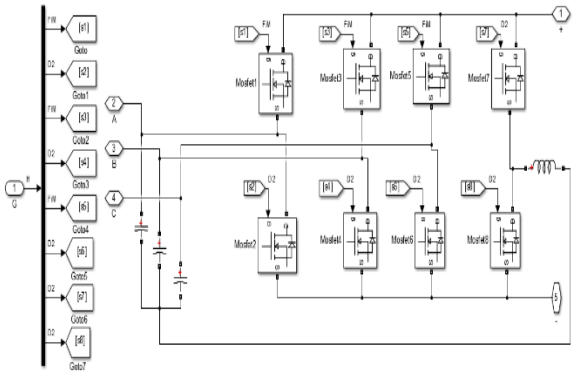

Fig.5 SIMULINK Model of 3-Phase 4-Leg Grid Interfacing Inverter.

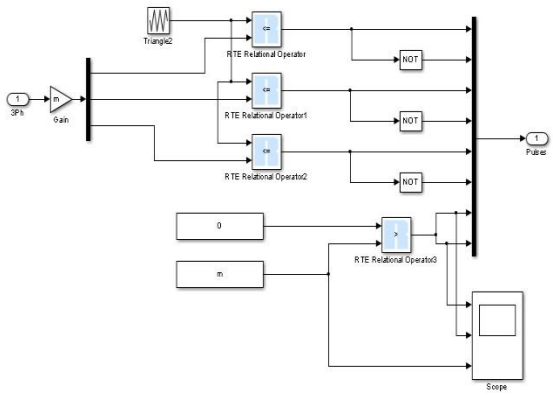

Fig.6 SIMULINK Model of PWM Pulse

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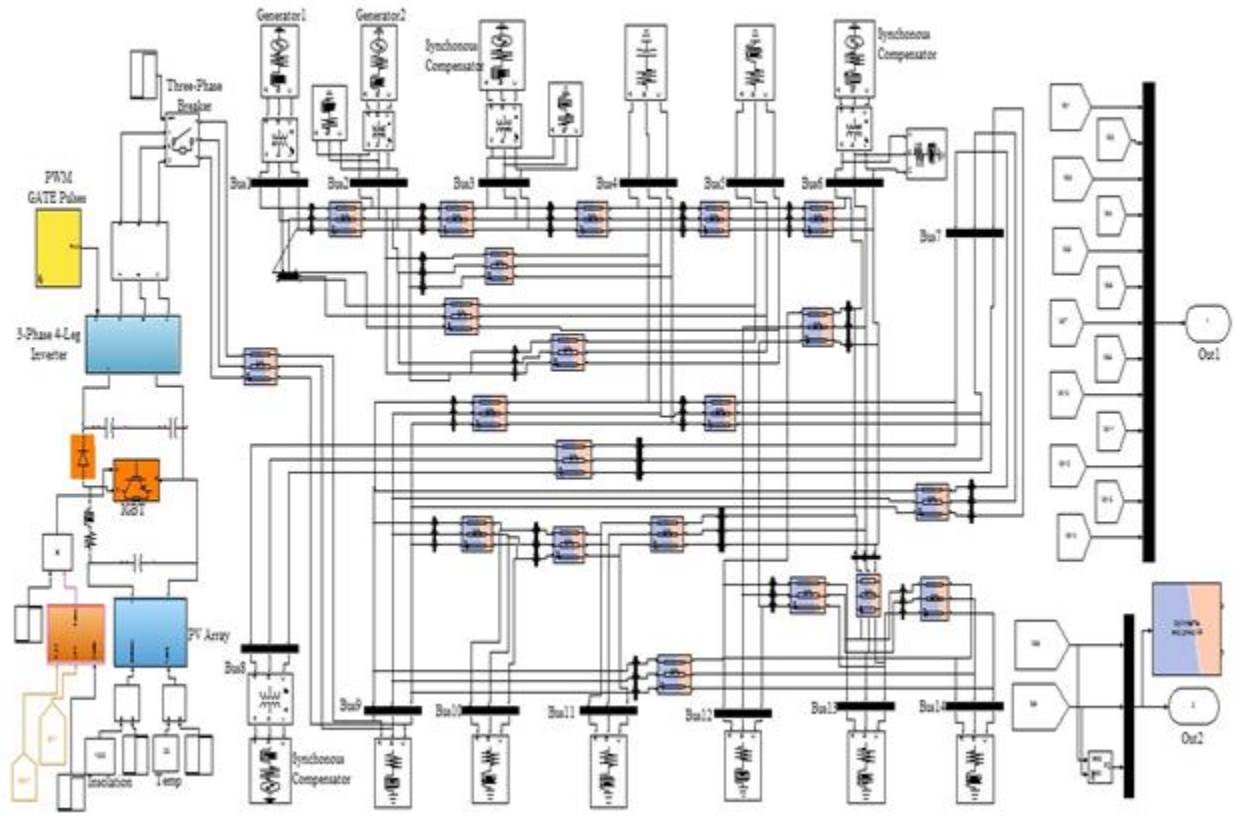

Fig. 7 Subsystem of SM_GRID

Fig. 7 and Fig. 8 are the modified model of grid and scope after OPAL-RT implication. And Fig. 9 is the overall OPAL-RT model which has basically two part Master and Console connected together.

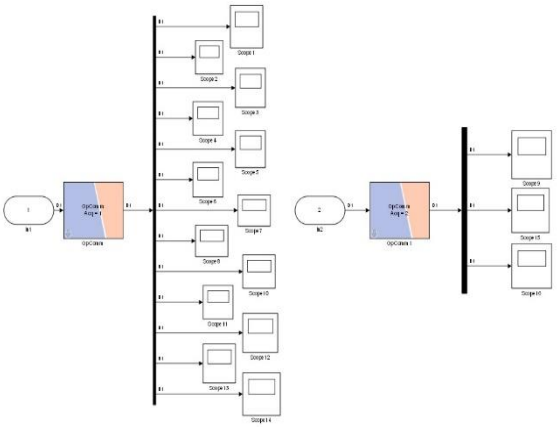

Fig. 8 Subsystem of SC_SCOPE

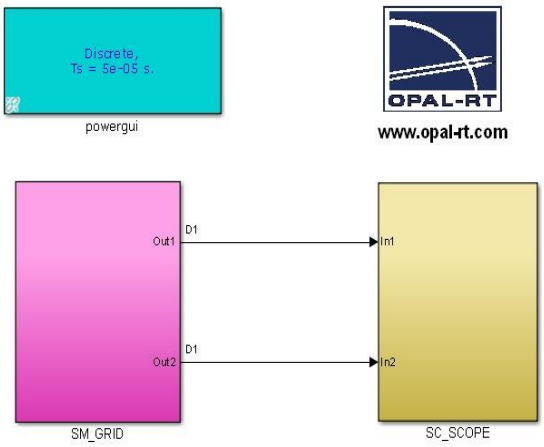

Fig. 9 OPAL-RT Model of PV Integrated System

Fig. 10 is the laboratory set-up of OPAL-RT implementation of PV model in which analog out of OP4510 is fed back to OP4510 analog input to get the result in console.

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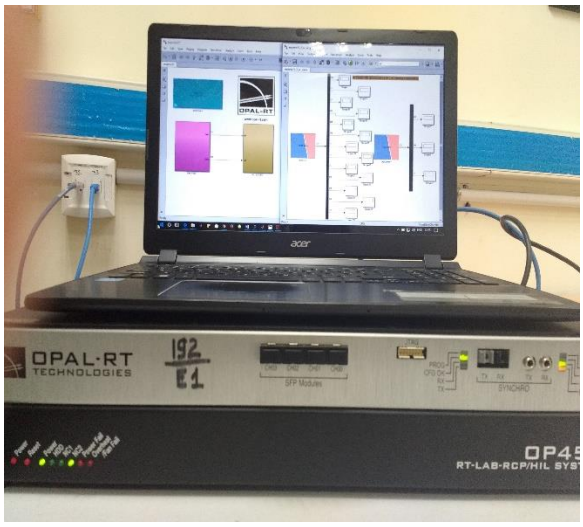

Fig. 10 OPAL-RT Model Interfaced with OP4510

V. Simulation Result

PV is interconnected to the existing IEEE 14 bus system at t=0.7s. The simulation result for bus no 9 of IEEE bus network is shown in Fig. 12. It can be seen that at t=0.7, transient condition has occurred and later it saturates with some disturbance in their waveform.

Fig. 11 is the confirmation pop-up window which is automatically generated by OPAL-RT after the model is built and loaded to OP4510.

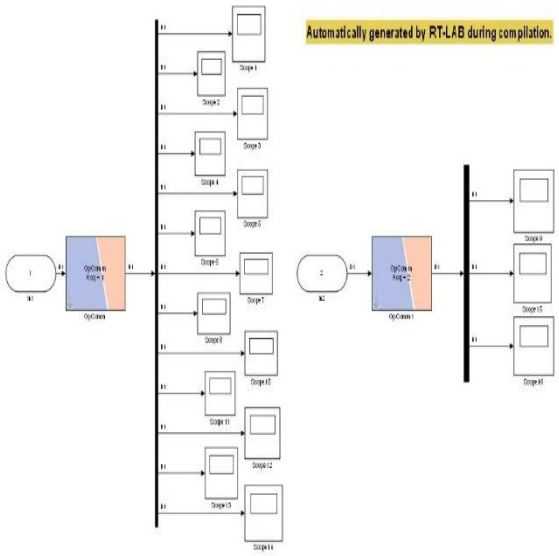

Fig. 11 New Console Automatically Generated by OPAL-RT

The OPWRITE block help to save all the measurement data of SC_SCOPE which is later plotted and analyzed.

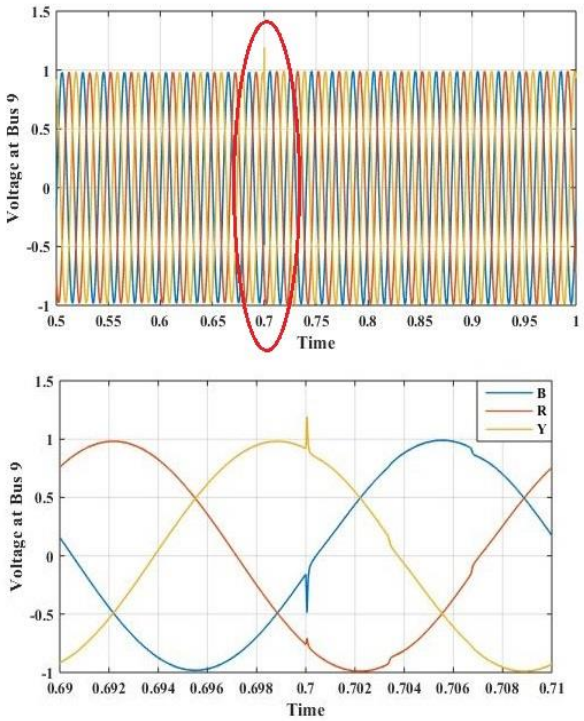

Fig.12 Voltage Waveform at Bus 9

Fig. 13 shows the voltage magnitude (pu) of all buses of IEEE 14 bus network obtained from SIMULINK result, OPAL-RT result and by the Newton Rapshon (N.R) method and their relative error is shown in Fig. 14.

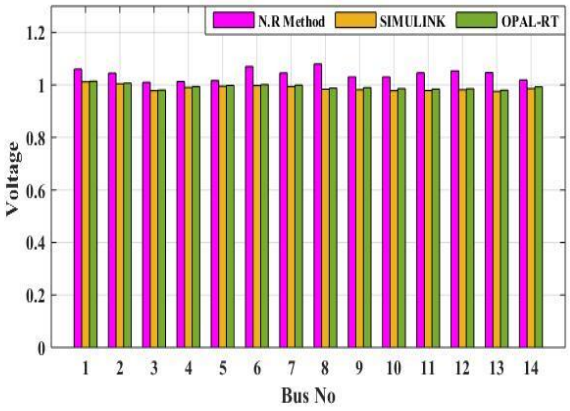

Fig.13 Voltages at Different Bus

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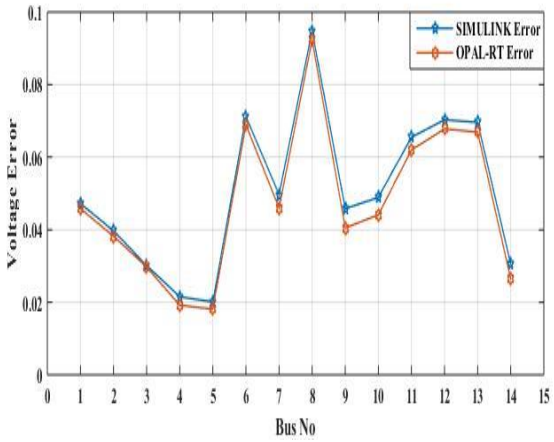

Fig.14 Voltage Error

From Fig.14 it is seen that the difference in voltages of both MATLAB/SIMULINK and OPAL-RT. It shows the error in voltage at each bus is less. This validate the proposed model.

Active and Reactive power flow through each bus is analyzed. Fig.15 shows power flow at bus 9 having transient at t=0.7 when RES is integrated and a slight difference with fluctuation after interconnection.

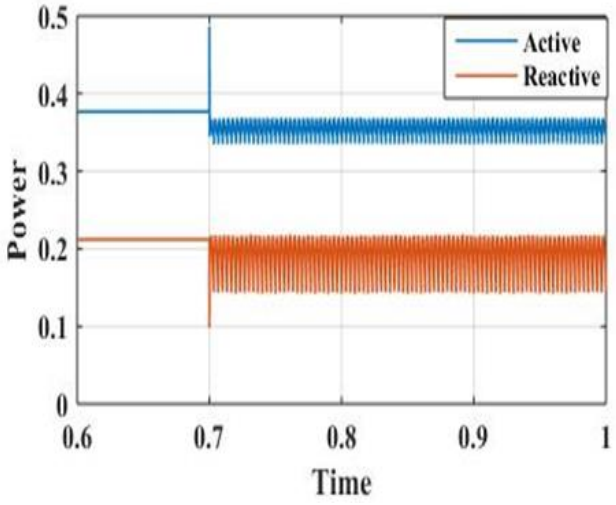

Fig.15 Active and Reactive power flow at Bus

Fig. 16 is shown represents that the voltage across dc link of the RES is constant which is desired for RESs like PV sources.

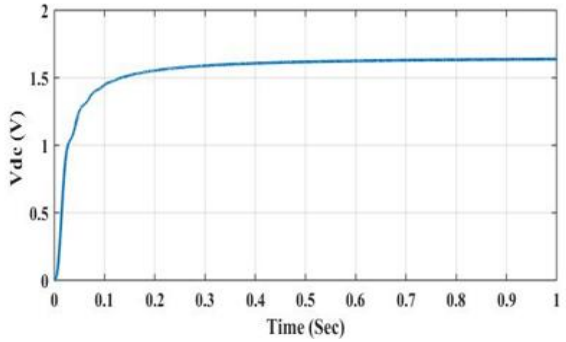

Fig.16 Voltage across dc Link

Fig. 17 is the current fed to grid from RES. Before 0.7s, the current fed from PV is zero then after circuit is made at the instant of 0.7s, sinusoidal waveform is generated by interfacing inverter.

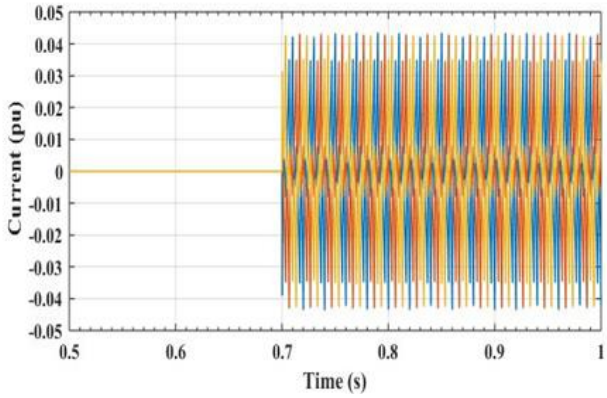

Fig. 17 Current Fed to Grid from PV

FFT analysis of voltage waveform at bus 9 for one cycle is analyzed in Fig.18 and the result is shown in Table 1.

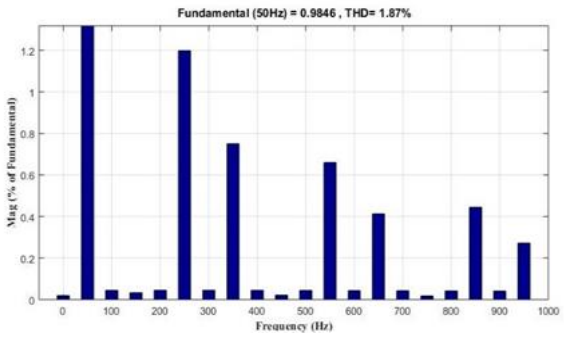

Fig. 18 FFT Analysis of Voltage at Bus 9

Table I
FFT Analysis

Sampling Time	50e-06 s
DC component	0.001887
THD	1.87 %
Fundamental	100.00 %
3rd Harmonics	0.03 %
5th Harmonics	1.20 %
7th Harmonics	0.75 %
9th Harmonics	0.02 %

From FFT analysis it is seen that THD is 1.87 % (less than 5 %) which is in permissible limit which also validate the proposed model.

VI. CONCLUSION

This paper has presented an interconnection model of PV system to existing IEEE 14 bus network using 3-phase 4-leg interfacing inverter while maintaining voltage profile of the distributed network. From the simulation result and OPAL-RT implementation of the model, it can be concluded that 3-phase 4-leg grid interfacing inverter can be effectively utilized for existing bus network interconnection maintaining voltage profile of the network.

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