International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 7, Issue 6, June 2017)

Design and Simulation of Nano Scale FIN FET using Silvaco TCAD

Kamal Prakash Pandey[1], Anil Kumar[2], A.K. Jaiswal[3]
[1]Research scholar, [2]Assistant Professor, [3]Professor, Department of ECE, SHUATS, Allahabad, UP- India.

***Abstract*- We present design and simulation of a single gate Fin-FET structure on the SOI substrate using Silvaco TCAD. A 45 nm channel length Fin-FET structure is compared with conventional MOSFET structure having same channel length. Different structural and process parameters such as length, width, height, dielectric thickness, doping etc has been optimized for designing the Fin-FET. The simulated structure shows the threshold voltage of 0.37643; lower DIBL, higher drain saturation current and improved parameters as compared to the conventional MOSFET structure.**

***Keywords*- DIBL, Fin-FET, MOSFET, SOI.**

I. Introduction

Discovery of first transistor in 1947 at Bell laboratory brings revolution in electronics and semiconductor industries. In the past six decades, [1] following the Moore's law, the semiconductor industry has emerged as the most essential part for all the organizations. [2] This microelectronics revolution has been intimately connected with advances in device structure, material science and technology. The complexity has increased from single transistor to integrated circuits to large scale integration to very large scale integration where entire subsystems are placed on a single chip. [3] The development in epitaxial growth technology allows precise control of layer thickness, composition and doping profiles on atomic scales. MOSFETs have been scaled down over the years and reaches to 11nm by 2016. [4] The scaling down of transistors give advantages like improvement in circuit speed (performance) and decrease in cost of implementation per function.[5]But further scaling of devices will face increasing difficulties due to increased leakage current, Drain Induced Barrier Lowering (DIBL), drain punch through, hot electron effect, mobility saturation, surface scattering etc. [6]

To further scale down devices innovations in technology like changes in material or the device structure needs to be done. Various non-classical MOSFET structures have been introduced for proper scaling. [7] Non-classical MOSFET structures include transport-enhanced MOSFETs, ultra-thin body SOI MOSFETs, source-drain engineered MOSFETs and multiple gate FETs. These non-classical structures offer various advantages like high mobility, better subthreshold slope, reduced SCE and DIBL.

Fin-FET is one such device that is made on ultra-thin body SOI substrate. It is a novel structure that uses gate all around the substrate for reducing the SCEs. It is constituted on very thin SOI substrate which is fully depleted. As it is a thin body structure it does not require heavy channel doping but the channel region is made thin to reduce leakage current. It can be considered as a multi gate structure because the gate covers the substrate from two or three sides for better electrostatic control. [8-10]

In this paper, a 45 nm Fin-FET structure has been simulated using Silvaco TCAD and compared with the conventional MOSFET. Different structural parameters such as threshold voltage, transconductance, DIBL, etc. has been calculated and well compared with the conventional MOSFET.

II. Design Approach

Silvaco TCAD simulation tools have been used for the designing of Fin-FET and MOSFET structures. The structures have been defined using Devedit 3D and the device simulation has been done on the Atlas tool. The simulation results suggest that Fin-FETs have much improved parameters as compared to a conventional MOSFET structure. The effect of Fin width on the Fin-FET transfer characteristics has been studied next. Fin-FET of Fin width 10nm, 20nm, 30nm has been simulated. Increasing Fin width leads to structure with higher effective channel widths. These structures have lower source/drain resistances and hence higher value of normalized drain current. As the channels in a Fin-FET are also vertically oriented, increasing the height of the fin also results in increased effective width of structures. This kind of structure is called a Tall Fin-FET structure. A tall Fin-FET structure does not have very high value of normalized drain current but shows better value of DIBL and subthreshold slope. If channel width and height are scaled down further the result is a nano-wire Fin-FET device. Such a device has very small cross-section and will be used when channel lengths are scaled further. It has been compared to a gate all around nano-wire structure.

Also finally channel engineering has been attempted to achieve better DIBL. Halo doping is known to reduce DIBL in both conventional and SOI structures.

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 7, Issue 6, June 2017)

Here different halo doping profiles have been studied to see their effects on DIBL in both 10nm and 30nm Fin width Fin-FET. The doping of the halo region has been varied to see the effect of changing the halo doping concentration on DIBL. At the same time the effect of halo doping on I_D and g_m has also been studied. Halo doping has been shown to improve the device characteristics.

III. Structure

A Fin-FET is a variation in double gate MOSFET where silicon substrate is made vertical and controlled by self-aligned gates [11]. It consists of ultra-thin Si substrate which helps in controlling the Short Channel Effects. It offers advantage over the double gate structure because the gates are self-aligned and the process and layout is similar to conventional MOSFET. [12] A Fin-FET structure is made by turning the silicon body on its side and thus creating the look of a fish's dorsal fin. Gate electrode has been created on both side of the silicon substrate. The problem of alignment faced in double gate structure is solved in this kind of structure because the entire gate is defined at the same time. Two possible structures of Fin-FET with single gate and multiple gates are shown in figure1 (a) and (b).

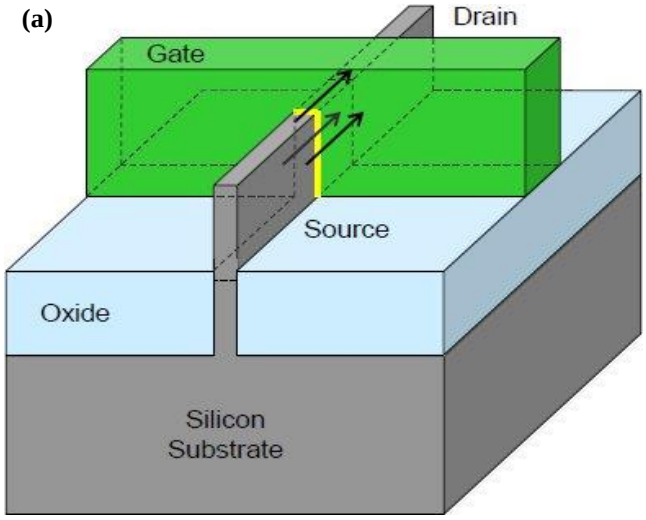


Figure 1. (a) Single gate Fin-FET, (b) Multi-gate Fin-FET.

In a Fin-FET there are three surfaces for current to flow, one at the top of channel and two at the side walls. The mobility along these surfaces are different. The drain current of a Fin-FET has been derived in [13]. The Drain current for a device is given by gradual channel approach and is given by:

$$I_D = -\mu W \frac{dV}{dZ} Q_{inv}(Z)$$

Here Z is the direction of current flow, μ and W are effective mobility and channel width respectively, Q_{inv} is the inversion charge density and $\frac{dV}{dZ}$ represents the lateral electric field. The total drain current is given by the addition of the current along the three surfaces as given by:

$$I_{D_{Total}} = I_{D_{top}} + 2 \times I_{D_{sidewall}}$$

Mobility is different for top and the sidewalls. Assuming identical gate length and oxide capacitances Drain Current can be given as follows:

$$I_{D_{Total}} = -\mu_{eff} W_{Total} \frac{dV}{dZ} Q_{inv}(z)$$

The effective mobility μ_{eff} is given by:

$$\mu_{eff} = \frac{\mu_{top} W_{FIN} + 2 \times \mu_{sidewall} H_{FIN}}{W_{FIN} + 2 \times H_{FIN}}$$

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 7, Issue 6, June 2017)

The effective width is given by:

$$W_T = W_{FIN} + 2 \times H_{FIN}$$

In the weak inversion region the current is given by the following exponential relation:

$$I_{drain} = I_o \times e^{\frac{V_{gate}}{nKT/q}}$$

Here I_o represents the current at zero gate voltage. The above equation can be used to find the subthreshold slope (S).

The transconductance parameter β is given by:

$$\beta = \frac{W_T}{L}\mu_{eff}C_{eff}$$

Here C_{eff} denotes the effective insulator capacitance per unit area. It accounts for both the top and sidewall capacitance. For a very thin dielectric layer capacitance does not depend on the crystal orientation and hence C_{eff} can be easily defined by the equivalent oxide thickness. The channel thickness cannot be scaled below a certain level. The channel thickness cannot go below 5nm because after that the intrinsic transconductance is strongly affected by the source resistance. [14, 15] In ATLAS for physically-based device simulation the following have to be provided:

1. The physical structure that needs to be simulated
2. The physical models that have to be used and
3. The bias voltages that have to be provided on electrodes for electrical characterization.

These are provided in form of input (Structure files and Command files) to the ATLAS device simulator. It gives output in the following form:

1. *Runtime Output*- it shows the progress of simulation and gives the error and warning messages.
2. *Log File*- it stores the terminal voltages and current from the analysis.
3. *Solution File*- it stores both 2D and 3D data which give the solution variables at a given bias point.

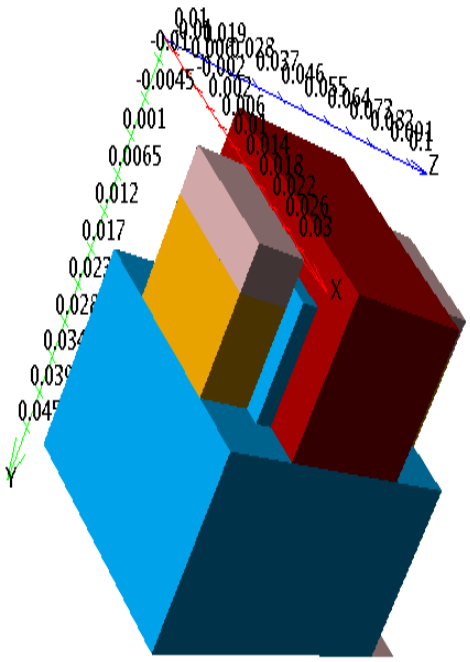
DEVEDIT 3D is a part of Silvaco TCAD tool. It is used to define the device. The meshes can also be defined on this tool. The defined structure is simulated on ATLAS.TONYPLOT is a post processing tool. It can be used with any simulator. It is used for examining data files. Numerical solution techniques also have to be specified. There are three types of solution technique

1. *GUMMEL (Decoupled)* - it solves for each unknown individually keeping other variables constant.
2. *NEWTON(Coupled)*- it solves the entire system of unknowns together
3. *BLOCK*- it solves few equations fully coupled and others de-coupled.

IV. Simulation And Result

A 3-dimentional Fin-FET structure has been defined using the DEVEDIT 3D. The results have been simulated using ATLAS simulator. Both the conventional MOSFET 3D and Fin-FET structures as defined using DEVEDIT-3D are shown in figure 2 (a) and figure 2 (b) respectively. The effective channel width of both the structures has been kept the same.

(a)



International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 7, Issue 6, June 2017)

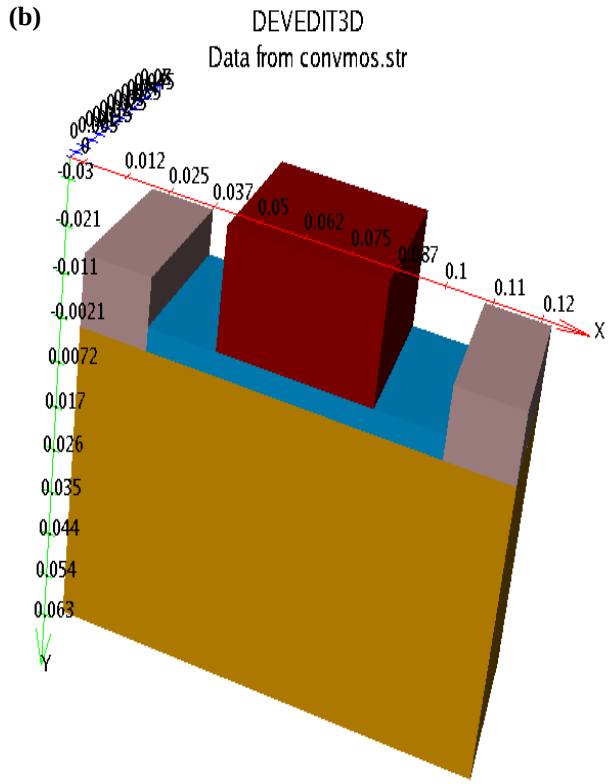


Figure 2. (a). Fin-FET structure for (Fin width = 20nm), (b).Conventional MOSFET

In a Fin-FET structure, we have Silicon- on- Insulator Substrate on which the device is fabricated. Silicon- on-Insulator substrate consists of a layer of Si on which SiO_2 is grown. Above this there is a layer of silicon on which the device is actually fabricated. This substrate is doped with Boron for making n-channel MOSFET. The source/drain regions are doped with Arsenic. The dielectric thicknesses on the top and sidewalls have been kept the same.

Conventional MOSFET structure of 45nm channel length is simulated for comparison with the Fin-FET structure. The Fin-FET and Conventional MOSFET device parameters as defined by our structure is given in Table 1 and the front view is given in figure 3 (a) and (b) respectively.

Table 1:
Structural Parameters for Fin-FET and Conventional MOSFET.

	FIN-FET	CONVENTIONAL MOSFET
Channel Length	45 nm	45 nm
Channel Width	50nm	50nm
Fin width	20nm	-
Fin height	15nm	-
Dielectric Thickness	3nm	3nm
Substrate Doping	1 X 10^{17} cm^{-3}	1 X 10^{17} cm^{-3}
Source/Drain Doping	1 X 10^{21} cm^{-3}	1 X 10^{21} cm^{-3}
GateWork function	4.65 eV	4.65 eV

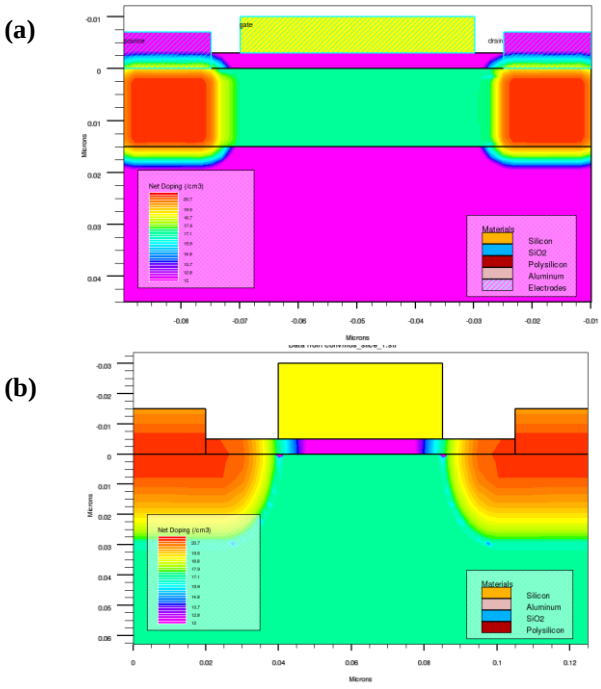


Figure 3. (a) Fin-FET doping profile, (b). Conventional MOSFET doping profile.

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 7, Issue 6, June 2017)

From the simulated Fin-FET and Conventional MOSFET structures, threshold voltage vs. drain voltage parameter was extracted as shown in figure 4.

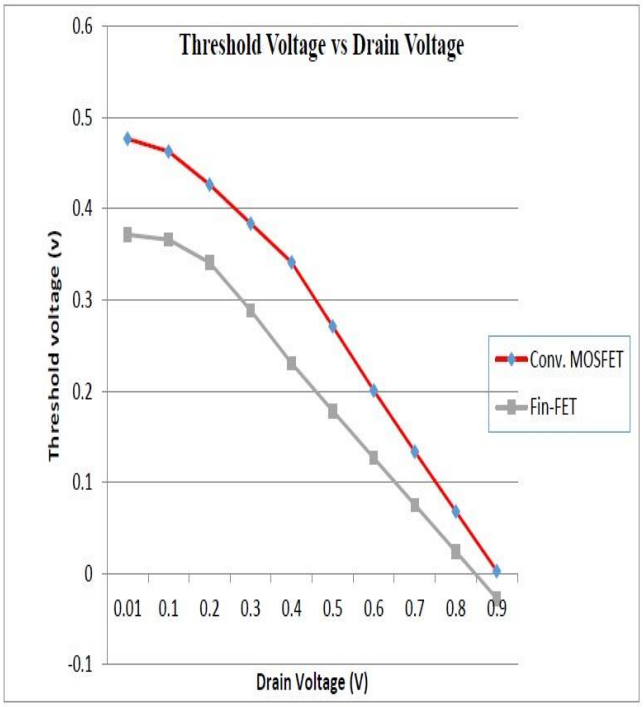
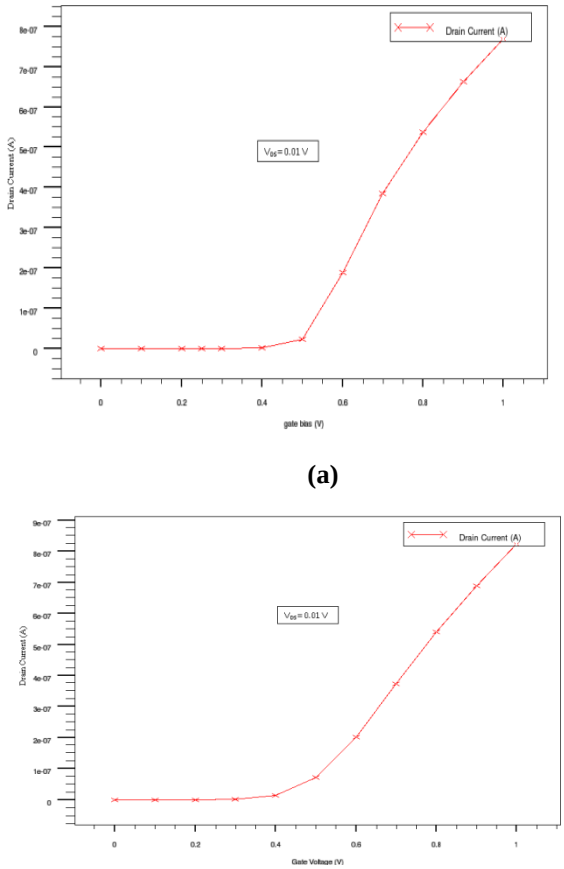


Figure 4: Plot of Threshold Voltage vs. Drain Voltage.

The designed Fin-FET shows lower threshold voltage as compared to the conventional MOSFET. Threshold voltage decreases with increase in the drain voltage due to drain induced barrier lowering effect. figure 5 (a) and (b) shows the drain current vs. gate voltage plot of Fin-FET and conventional MOSFET respectively. V_T, β and θ have been extracted from this curve.



(a)

(b)

Figure 5: Drain Current vs Gate Voltage plot for 20nm fin width Fin-FET. Figure Error! No text of specified style in document.**-1: Drain Current vs Gate Voltage plot for Conventional MOSFET.**

The mobility degradation parameter θ is more for Fin-FET than for conventional MOSFET structure. This is because the mobility degradation in a Fin-FET has been found to increase because of increase in transverse electric field. Figure 6 (a) and (b) shows the drain current vs. drain voltage plot at different gate voltages for Fin-FET and conventional MOSFET respectively.

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 7, Issue 6, June 2017)

(a)

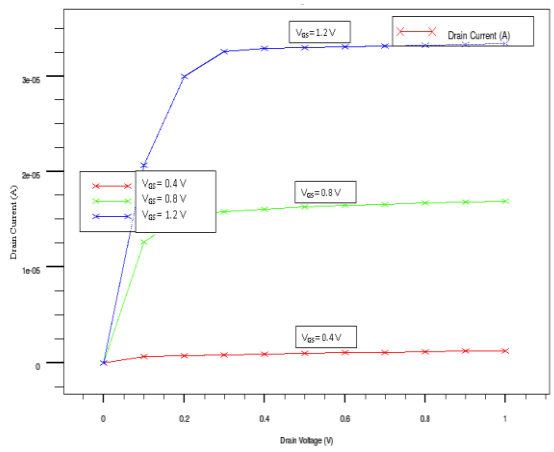


Figure 6. Drain Current vs Drain Voltage Graph for (a) 20nm Fin width Fin-FET

(b)

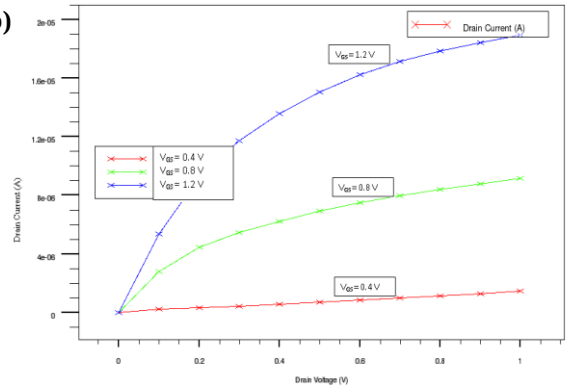


Figure 6. Drain Current vs Drain Voltage Graph for (b) Conventional MOSFET

In Fin-FET or any other multiple gate structure the substrate doping can be kept low and the Short Channel Effects can be controlled as the devices are scaled. Because of lower doping concentration of the substrate the mobility is less affected by scattering. Here the doping of substrate has been kept same in case of both Fin-FET and conventional MOSFET for comparison purpose. Still it can be seen that the g_m for Fin-FET is more than that of the conventional bulk MOSFET structure. In a Fin-FET the active Device width is not just the fin width but twice the fin height plus the fin width. Hence the active channel width is increased in Fin-FET. In a Fin-FET structure there is volume inversion of the entire device as in a fully depleted SOI double gate structure.

This leads to an increase in the number of minority carriers. Surface-induced scattering and surface interface charge is reduced because of increase in volume of the channel. This also results in increased transconductance and effective mobility. The increased volume hence leads to increase in drain current and g_m.

(a)

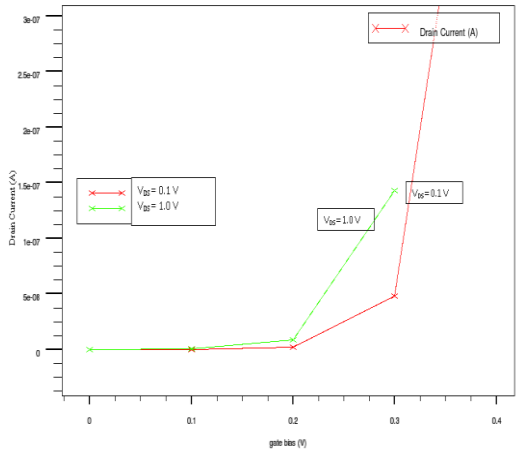


Figure 7. (a) Effect of DIBL on 20nm Fin width Fin-FET

(b)

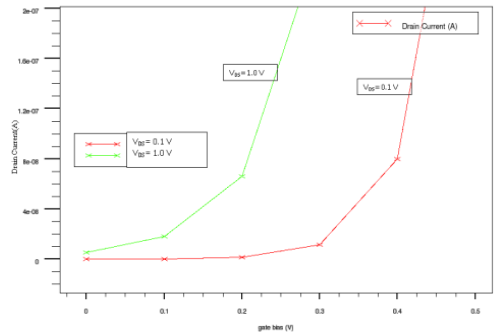
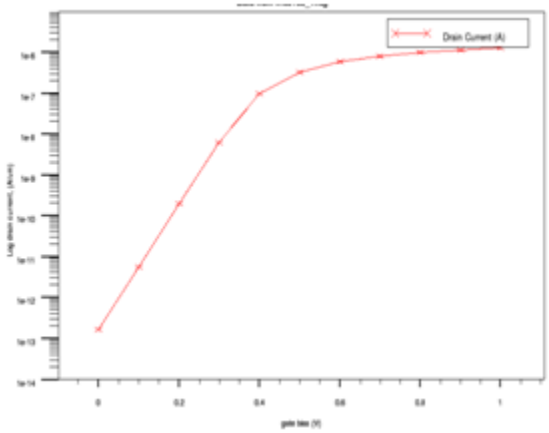


Figure 7. (b). Effect of DIBL on conventional MOSFET

The effect of DIBL on Fin-FET and Conventional MOSFET is shown in figure 7 (a) and (b) respectively. DIBL for Fin-FET is less than for a conventional MOSFET structure. As already stated in small channel MOSFETs the potential barrier of the channel region is controlled by both the gate to source voltage and drain to source voltage. Increasing the drain voltage leads to reduction in potential barrier of the channel this is known as DIBL. Use of thin substrates helps in reducing the DIBL.

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 7, Issue 6, June 2017)

(a)



(b)

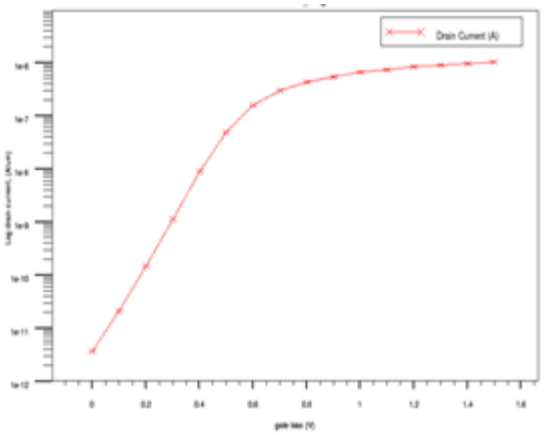


Figure 8. (a) Subthreshold current plot for 20nm Fin width Fin-FET, (b) Subthreshold current plot for Conventional MOSFET.

Figure 8 (a) and (b) give the subthreshold plot for Fin-FET and conventional MOSFET respectively. The subthreshold slope for Fin-FET is increased. This results in faster switching for the devices.

The comparison between different Fin-FET and Conventional MOSFET parameters is given by

Table 2 :
Comparison between 45nm Conventional MOSFET and Fin-FET.

PARAMETERS	CONV. MOSFET	Fin-FET
Threshold Voltage (V)	0.477337	0.37643
β (A/V^2) (X 10^{-5})	17.1164	44.6
DIBL (mV/V)	94.94	44.9144
Subthreshold Slope(mV/dec)	52.333	73.2012
g_m ($\mu S/\mu m$)	550	800
θ	0.173595	0.551135
I_{DSat} (V_{GS} =1.2V)	20 µA	33 µA
I_{DSat} (V_{GS} =0.8V)	9 µA	16.5 µA
I_{DSat} (V_{GS} =0.4V)	0 µA	1.0 µA
Normalized I_D (V_{GS} =1.2V)	400 µA/ µm	660 µA/ µm
Normalized I_D (V_{GS} =0.8V)	180 µA/ µm	330 µA/ µm
Normalized I_D (V_{DS} =0.4V)	0 µA/ µm	20 µA/ µm

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 7, Issue 6, June 2017)

V. Conclusion

Fin-FET structure is simulated and compared to a conventional MOSFET structure having the same effective width. It is shown that the Fin-FET structure has lower threshold voltage than a conventional MOSFET structure. A Fin-FET also has increased saturation drain current and g_m as compared to a conventional structure. In the structures simulated here the Fin-FET has a Fin width of 20nm whereas the conventional MOSFET has a width of 50nm.In the Fin-FET structure the gate has far superior control over the channel region. Hence DIBL is much reduced in the Fin-FET structure. The mobility is reduced in Fin-FET because of increase in surface scattering. This is mainly because of increase in transverse Electric Field. Overall various advantages of Fin-FET over conventional MOSFET structure were demonstrated in this work.

REFERENCES

[1] Braun, Ernest, and Stuart MacDonald. Revolution in miniature: The history and impact of semiconductor electronics. Cambridge University Press, 1982.

[2] Tushman, L. Michael, and A. Charles O'Reilly. "The ambidextrous organizations: Managing evolutionary and revolutionary change." California management review 38.4 (1996):pp. 8-30.

[3] Eichelberger, B. Edward, and T. W. Williams. "A logic design structure for LSI testability." Proceedings of the 14th design automation conference. IEEE Press, 1977.

[4] Neisser, Mark, and S. Wurm. "ITRS lithography roadmap: 2015 challenges." Advanced Optical Technologies 4.4 (2015):pp. 235-240.

[5] Horowitz and Mark. "Scaling, power, and the future of CMOS." Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International. IEEE, 2005.

[6] D'Agostino, Fabio, and D. Quercia. "Short-channel effects in MOSFETs." Introduction to VLSI design (EECS 467) (2000).

[7] A. B. Bhattacharyya. "Non Classical MOSFET Structures." Compact Mosfet Models for VLSI Design: pp. 383-413.

[8] D. K. Sadana, D. M. Fried, E. J. Nowak, B. A. Rainey "Fin FET devices from bulk semiconductor and method for forming." U.S. Patent No. 6,642,090. 4 Nov. 2003.

[9] E. J. Nowak, J. Edward, I. Aller and T. Ludwing. "Turning silicon on its edge [double gate CMOS/FinFET technology]." IEEE Circuits and Devices Magazine 20.1 (2004):pp. 20-31.

[10] Z. Cheng, E. A. Fitzgerald, and D. Antoniadis. "FinFET structure and method to make the same." U.S. Patent No. 7,304,336. 4 Dec. 2007.

[11] X. Huang, Wen-Chin Lee, C. Kuo, D. Hisamot, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi, Kazuya Asano, Vivek Subramanian, Tsu-Jae King, J. Bokor and C. Hu "Sub 50-nm FinFET: PMOS" in IEDM Tech. Dig. pp. 67-70.

[12] V. X. Huang, W. C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi, K. Asano, V. Subramanian, T.J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PFET," in Tech. Digest IEDM 1999, Washington, DC, pp. 67–70.

[13] V. V. Iyengar, A. Kottantharayil, F. M. Tranjan, M. Jurczak, K. De Meyer, "Extraction of the Top and Sidewall Mobility in FinFETs and the Impact of Fin-Patterning Processes and Gate Dielectrics on Mobility " in IEEE Transactions on Electron Devices, pp. 1177 – 1184.

[14] D. J. Frank, S. E. Laux and M. V. Fischetti, " Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?" in IEDM,1992 pp 553.

[15] T. Dutta, S. Dasgupta, "Scaling issues in nanoscale double gate FinFETs with source/drain underlap" in Computers and Devices for Communication, 2009. CODEC 2009. 4th International Conference on , pp.1-4.